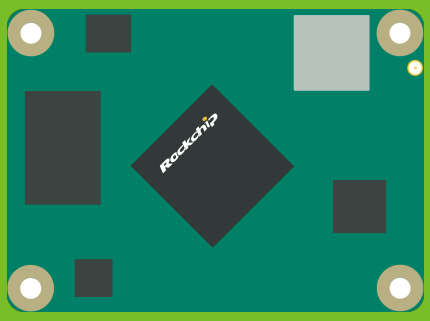
Radxa Compute Module 3

A feature rich embedded system-on-module

Revision 1.1



Radxa Computer

2023-06-02

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Version	Date	Changes from previous version
1.0	24/05/2023	First version
1.1	02/06/2023	Update Information

2 Introduction

2.1 Overview

The Radxa Compute Modules 3 (Radxa CM3) are optimized for integrated designs, utilizing a System-on-Module architecture. The Radxa CM3 combines the processor, memory, wireless, Bluetooth, and optional integrated heat shield, offering a compact and efficient solution. Storage may also be included, depending on the model (refer to Table 1 for a summary). It is important to note that the Radxa CM3 requires a compatible carrier board for proper operation.

For a list of compatible devices to use with the Radxa CM3, please refer to Radxa Wiki.

Note:
Radxa CM3 has obtained certification as a component for use in Information Technology Equipment in certain countries. However, it is the responsibility of the system integrator to conduct testing and acquire any additional country-specific regulatory approvals, including all necessary system-wide certifications.

2.2 Hardware

The RADXA CM3 compute module is built upon the powerful RK3566 System on Chip (SoC) from Rockchip. The RK3566 is a Quad-core Cortex-A55 64-bit SoC operating at a clock speed of 1.8GHz, providing excellent performance for embedded computing applications.

With regard to memory, the CM3 module offers multiple options, including 1GB, 2GB, 4GB, or 8GB LPDDR4, allowing users to choose the variant that best suits their requirements.

Connectivity is a key aspect of the CM3 module. It supports optional wireless LAN, featuring 2.4GHz and 5.0GHz IEEE 802.11b/g/n/ac standards, along with Bluetooth 5.0 and BLE. Both onboard and external antenna options are available, ensuring reliable wireless connectivity. Furthermore, the module incorporates an onboard Gigabit Ethernet PHY for seamless wired network connectivity.

For peripheral connectivity, the CM3 module includes a diverse set of interfaces. It provides one high-speed USB 2.0 port and one USB 3.0 port with a data transfer rate of 5Gbps. Additionally, it features a PCIe 1-lane Host with Gen 2 support, enabling high-speed expansion capabilities. The module also offers two SATA ports, with one shared with USB 3.0 and the other shared with PCIe, facilitating efficient data storage.

The CM3 module boasts an array of video interfaces, including one HDMI port supporting resolutions up to 4K x 2K@60Hz. It also features one eDP (embedded DisplayPort) with four lanes operating at 2.7Gbps per lane, two MIPI DSI (Mobile Industry Processor Interface Display Serial Interface) ports with four lanes each operating at 1.6Gbps per lane, and one LVDS (Low Voltage Differential Signaling) port with four lanes (muxed with MIPI DSI0).

In terms of audio capabilities, the CM3 module offers LINEOUT, I2S, and supports microphone arrays utilizing PDM (Pulse Density Modulation) technology.

When it comes to multimedia processing, the module excels at decoding VP9, H.264, and H.265 video codecs at 4K@60Hz resolution. It also supports hardware encoding of H.264 and H.265 at 1080P@100Hz. The GPU of the RK3566 SoC enables OpenGL ES 3.2, OpenCL 2.0, and Vulkan 1.1, delivering efficient and powerful multimedia processing capabilities.

Powering the RADXA CM3 module requires a 5V DC input, ensuring easy integration with various power sources.

The module's connector consists of three 100P 0.4mm pitch Board-to-Board (B2B) connectors, offering secure and reliable connections.

The RADXA CM3 module is designed for longevity, with a planned production lifetime extending until at least September 2029, providing customers with long-term availability and support.

Overall, the RADXA CM3 module based on the RK3566 SoC delivers a comprehensive solution for a wide range of applications, including graphics-intensive tasks, imaging, machine vision, audio processing, video applications, and safety-critical systems. It provides a variety of interfaces, from basic GPIOs and industry-standard I2C and SPI buses to high-speed USB 3.0, PCI Express, and SATA interfaces. The module's HDMI and LVDS interfaces simplify the connection of high-resolution displays. Additionally, the module incorporates Wi-Fi 802.11a/b/g/n/ac and Bluetooth v5.0 (BR/EDR/BLE) with pre-certification for FCC (US), CE (Europe), and IC (Canada).

2.3 Feature Summary

Table 2: *Radxa CM3 feature summary*

Features	Description
Form factor:	55 mm × 40 mm
Processors:	Rockchip RK3566, Quad core Cortex-A55 (ARM v8) 64-bit SoC @ 1.8GHz
Memory:	1GB, 2GB, 4GB or 8GB LPDDR4 (depending on variant)
Connectivity:	• Optional wireless LAN, 2.4GHz and 5.0GHz IEEE 802.11b/g/n/ac wireless, Bluetooth 5.0, BLE with onboard and external antenna options • Onboard Gigabit Ethernet PHY • 1 × USB 2.0 port (highspeed), 1 x USB 3.0 port (5Gbps) • 1 × PCIe 1-lane Host, Gen 2 (5Gbps) • 2 x SATA ports, one shared with USB 3, one shared with PCIe • 50 × GPIO supporting
Video:	• 1x HDMI up to 4K x 2K@60HZ • 1x eDP four lanes, 2.7Gps per lane • 2x MIPI DSI four lanes, 1.6Gbps per lane • 1x LVDS four lanes(muxed with MIPI DSI0)
Audio:	• LINEOUT • I2S • PDM, support mic array
Multimedia:	• VP9/H.264/H.265 decode 4K@60HZ • H.264/H.265 encode 1080P@100HZ • OpenGL ES 3.2/OpenCL 2.0/Vulkan 1.1 GPU
Input power:	5V DC
Connector	3x 100P 0.4mm pitch B2B connector
Production lifetime:	Radxa CM3 will remain in production until at least Sep 2029

2.4 Block Diagram

Figure below is a block diagram of the major functional areas of Radxa CM3.

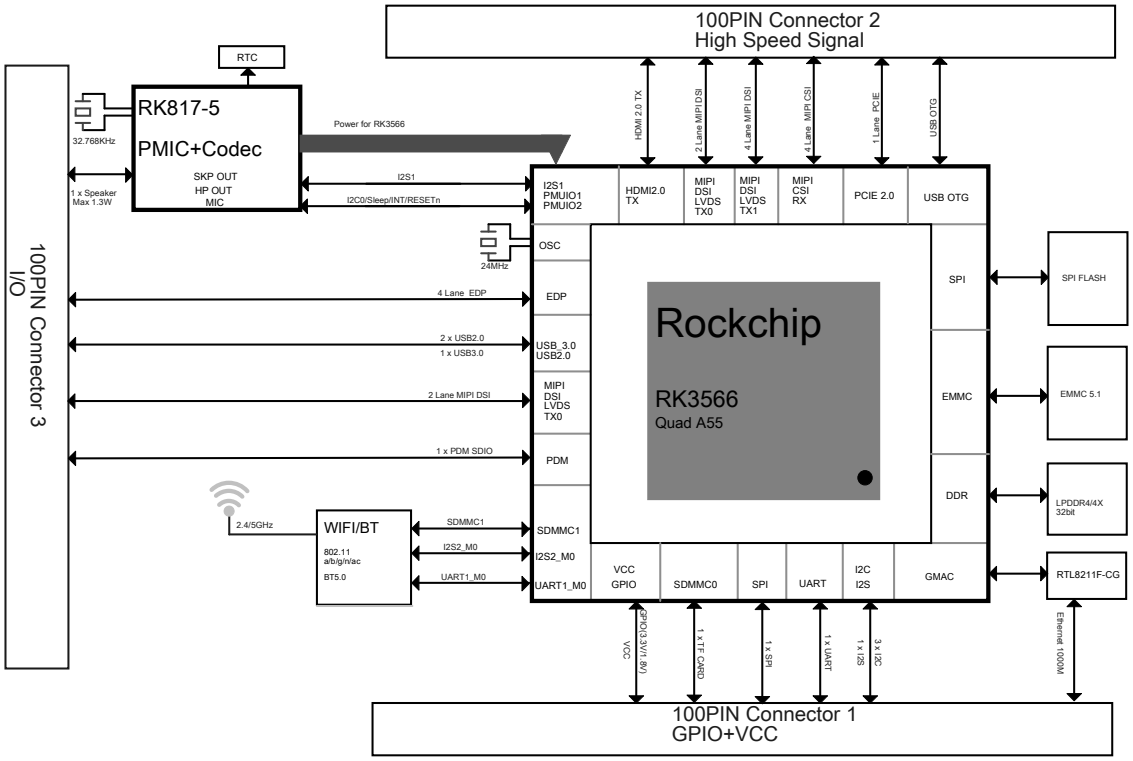

Figure 1: *Radxa CM3 Block Diagram*

2.5 Evaluation Board

To enhance your development experience with the Radxa CM3 compute module, Radxa offers a comprehensive range of peripherals and accessories. These include the Radxa CM3 IO board, Dual MIPI Cameras, 8-inch or 10-inch MIPI touch screen, 13.3-inch eDP LCD panel, power adapter, heatsink, antenna, and more. These peripherals are designed to facilitate module control and testing for seamless integration into your applications.

For convenient access to the design files of the Radxa CM3 IO board, they can be found on the Radxa Github. The CM3 IO board design files are available in Orcad or Altium Designer format, providing flexibility to work with different design tools as per your preference.

2.6 Compute Module Layout

The following figure displays the board layout of the Radxa CM3. Each connector and major component is labeled with a number or letter for easy identification. A description of each labeled item is provided in the table below the figure.

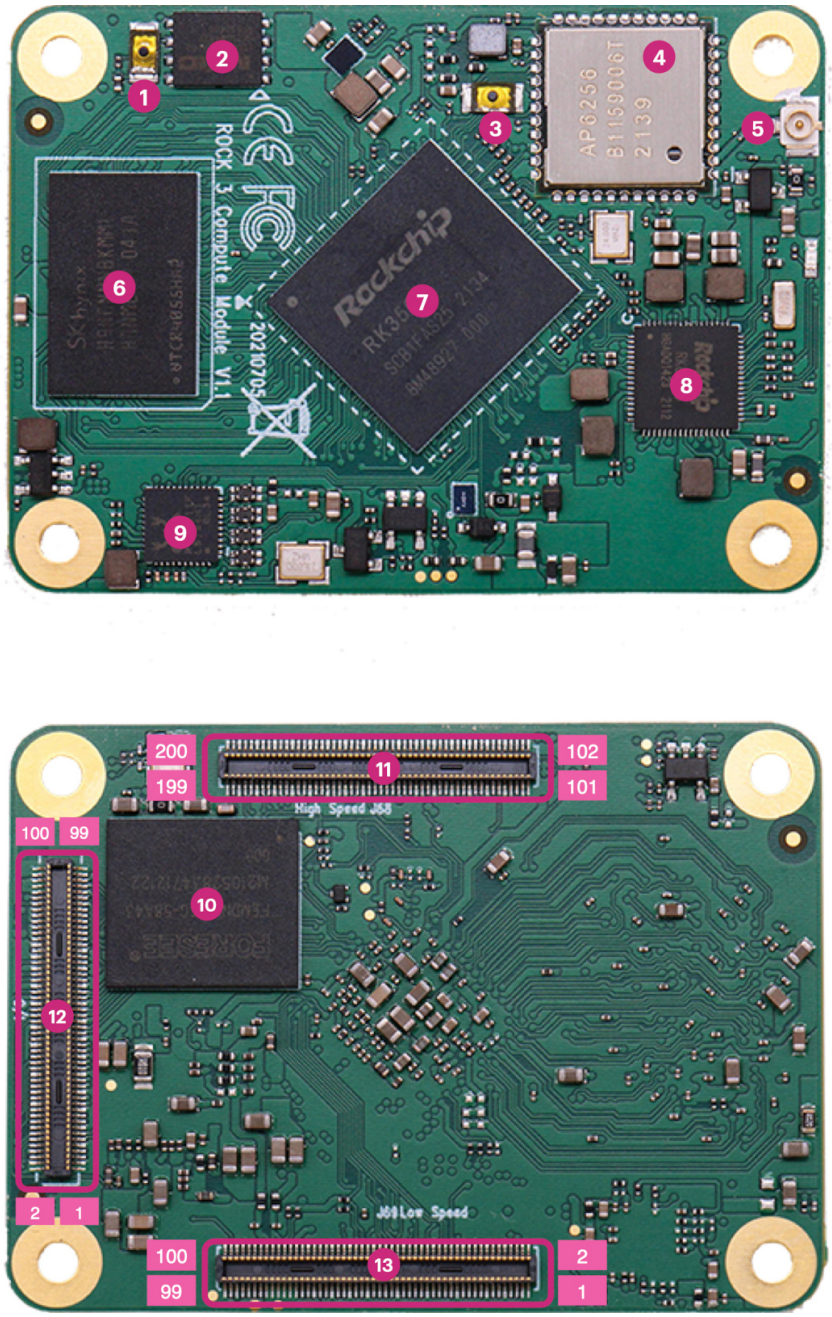

Figure 2: *Radxa CM3 Top and Bottom View*

Figure: Radxa CM3 Top and Bottom View

No.	Description	No.	Description
①	SPI Flash disable button	⑧	RK817-5 PMIC
②	SPI Flash	⑨	RTL8211F Ethernet PHY
③	eMMC disable button	⑩	eMMC chip (Not available on E0 SKU)
④	WiFi/BT module	⑪	B2B connector 2 (J68)
⑤	WiFi/BT antenna	⑫	B2B connector 3 (J1)
⑥	LPDDR4 DRAM chip	⑬	B2B connector 1 (J69)
⑦	RK3566 SoC		

Table: Components Description on the Radxa CM3

> **Note:** The specific components on the Compute Module may vary depending on the SKU. For example, the E0 SKU does not include the eMMC chip (No. ⑩).

2.7 Connector

The Radxa CM3 connects to the carrier board via a 3x 100-pin board-to-board (B2B) connector. The connector on the Radxa CM3 is a Hirose 100-pin DF40 Series *header* connector, specifically the DF40C-100DP-0.4V(51) model.

The corresponding connector on the carrier board is the *receptacle* connector, available in two different stack heights: 1.5mm and 3.0mm. The stack height determines the clearance space under the Radxa CM3. The following table provides the Hirose part numbers for the *receptacle* connectors and their corresponding stack heights:

Hirose P/N	Mating Stack Height	Clearance under Radxa CM3
DF40C-100DS-0.4V(51)	1.5mm	N/A (no components allowed)
DF40HC(3.0)-100DS-0.4V(51)	3.0mm	1.5mm

Table: Connector Part Numbers and Stack Heights

The Radxa CM3 features four mounting holes, each with a diameter of 3.5mm, for secure attachment to the carrier board. It is important to ensure that the mounting standoffs used match the mating connector's height (either 1.5mm or 3.0mm).

The Radxa CM3 IO board utilizes the 1.5mm board-to-board stack height connector.

Note:
The connector specifications and dimensions mentioned here are specific to the Radxa CM3 and may vary for other products.

3 Interfaces

3.1 Power Supply

3.1.1 Power Supply Pins

Radxa CM3 supports 5V DC input or battery input. The power output on the B2B connector can supply up to 200mA at +3.3V and 200mA at +1.8V peripherals.

Signal	Pin number	Power Input / Output	Typical Voltage	Voltage Range	Voltage Ripple	Typical Current
+5V_INPUT	(J69)pin77 79 81 83 85 87	Input for	5V	3.8V to 5.2V	100mV Vp-p	3A
GPIO_VREF	(J69)pin78	Input voltage select, connect to pin84/86 when use 3.3V, connect pin88/90 when use 1.8V	3.3V(default)	1.8V or 3.3V	50mV Vp-p	200mA
+3V3	(J69)pin84 86	Output	3.3V	3.3V	50mV Vp-p	200mA
+1V8	(J69)pin88 90	Output	1.8V	1.8V	50mV Vp-p	200mA
VCCIO_SD	(J1)pin92	Output	3.3V(default)	1.8V or 3.3V	50mV Vp-p	400mA
USB_5V_IN	(J1)pin94 96 98	Battery charging input	5V	3.8V to 5.2V	100mV Vp-p	500mA-3000mA
VCC_BAT-	(J1)pin78 80 82	Battery nagetive output	-	-	-	-
VCC_BAT+	(J1)pin84 86 88	Battery positive ouput	4.2V	4.1V to 4.45V	-	charging current 0.5A-3.5A
TS	(J1)pin90	Battery temperature detect input		0V to 5V	-	-

Warning:
When powering the CM3 from +5V_INPUT, do not power the USB_5V_IN at the same time, thus may damage other components on the CM3.

3.1.2 Power with DC source

When users are designing the baseboard, if powered by a DC power supply, they need to convert the power supply to 5V before connecting it to the +5V_INPUT pin on the CM3. On

the compute module, CM3 connects the +5V_INPUT rail to the VCC_SYS rail. The 'VCC_SYS rail acts as the primary power supply for the entire compute module.

The RADXA CM3 board features an RK817-5 PMU (Power Management Unit). When a **+5** V_INPUT signal is detected, the automatic power-on circuit of the RK817-5 is activated, initiating the automatic power-on process. The power-on sequence of the RK817-5 is fixed and cannot be adjusted.

When designing the baseboard, users do not need to be concerned about the fixed sequence of the RK817-5. Instead, the focus should be on correctly using VCCIO_SD and GPIO_VREF.

The SD card circuit interface uses VCCIO_SD for pull-up, but since it is already internally pulled up within the RK3566 chip, there is no need to use an external pull-up resistor. The GPIO_VREF can be selected as either **+3V3** or **+1V8** output from the Compute Module.

If the peripheral interface operates at 3.3V, choose **+3V3** for GPIO_VREF. Conversely, if the peripheral interface operates at 1.8V, choose the compute module's **+1V8** output for GPIO_VREF. It is essential to ensure that the peripheral interface level matches the chip interface level. The Compute Module's **+3V3** output is connected to VCC3V3_SYS and powers on in **SLOT3**. Similarly, the Compute Module's **+1V8** output is connected to VCC_1V8 and powers on in **SLOT2**. By selecting GPIO_VREF from either of these two voltages, the power-on sequence requirements can be met. If the custom baseboard needs to control the power-on sequence of other chips, it can be flexibly managed according to the specifications detailed in the chip's manual.

3.1.3 Power With Battery

The RADXA CM3 compute module is equipped with a Power Management Unit (PMU) that incorporates battery management functionality. The board-to-board (B2B) connector on the CM3 module has three signal connections: VCC_BAT+, VCC_BAT-, and the TS pin. When designing a baseboard, users only need to connect these three signals to their corresponding counterparts on the battery.

In the CM3 compute module, the TS pin of the battery is connected to the RK817-5 TS/GPIO pin. Changes in temperature can alter the resistance value of the internal thermistor in the battery, thereby affecting the voltage at the voltage dividing point. This voltage is then sent to the PMU chip for real-time monitoring and control processing.

The VCC_BAT+ signal on the CM3 compute module is connected to the BAT pin of the RK817-5. The RK817-5 manages charging and discharging operations through its internal and external MOSFETs. On the other hand, VCC_BAT- on the CM3 compute module is connected

in series with a sampling resistor. The ends of the sampling resistor are linked to the internal Gas Gauge of the RK817-5, enabling power statistics.

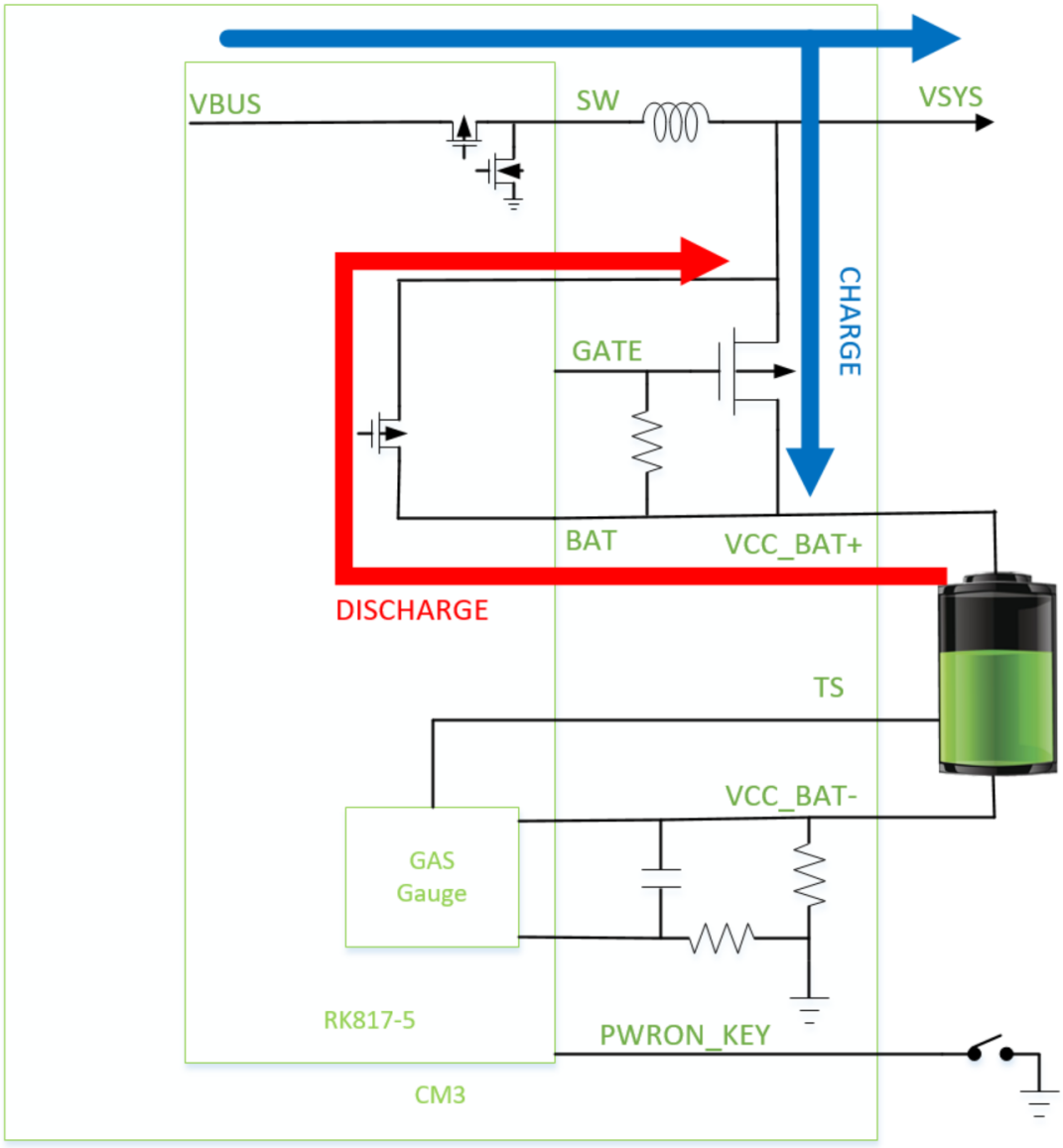

Figure 3: *Power With Battery*

Note:
When designing the baseboard, it is important to ensure that the traces for VCC_BAT+ and VCC_BAT- are as wide and short as possible. Additionally, the TS trace should be routed away from signals with strong interference and should be subject to ground shielding.

3.1.4 Power On Sequence

In the power-on sequence, VDDA0V9_PMU, VDDA_0V9, and VDD_LOGIC are part of **SLOT1** and are the first to power on. Following them, VCC3V3_PMU, VCCA1V8_PMU, VDD_NPU, VDD_GPU, and VCC_1V8 belong to **SLOT2** and power on in the second stage.

The power supply VDD_CPU is provided by an external DCDC and controlled by VCC3V3_PMU, powering on in **SLOT2** sequence. VCC1V8_DDR, VCC0V6_DDR, and VCC_DDR are part of **SLOT3** and power on in the third stage. **SLOT4** includes VCC3V3_SYS / VCC_3V3, VCCIO_SD, and VCC3V3_SD, which power on in the fourth stage of the sequence.

Once the power-on process is completed, the PMU generates a reset signal to reset the RK3566. The power sources VCCIO_ACODEC, VCC1V8_DVP, VCC2V8_DVP, and VDD1V2_DVP are typically off by default. They are activated later in the boot process by configuring the RK817-5 registers from software when they are required.

For more detailed information, please consult the RK817 User's Manual.

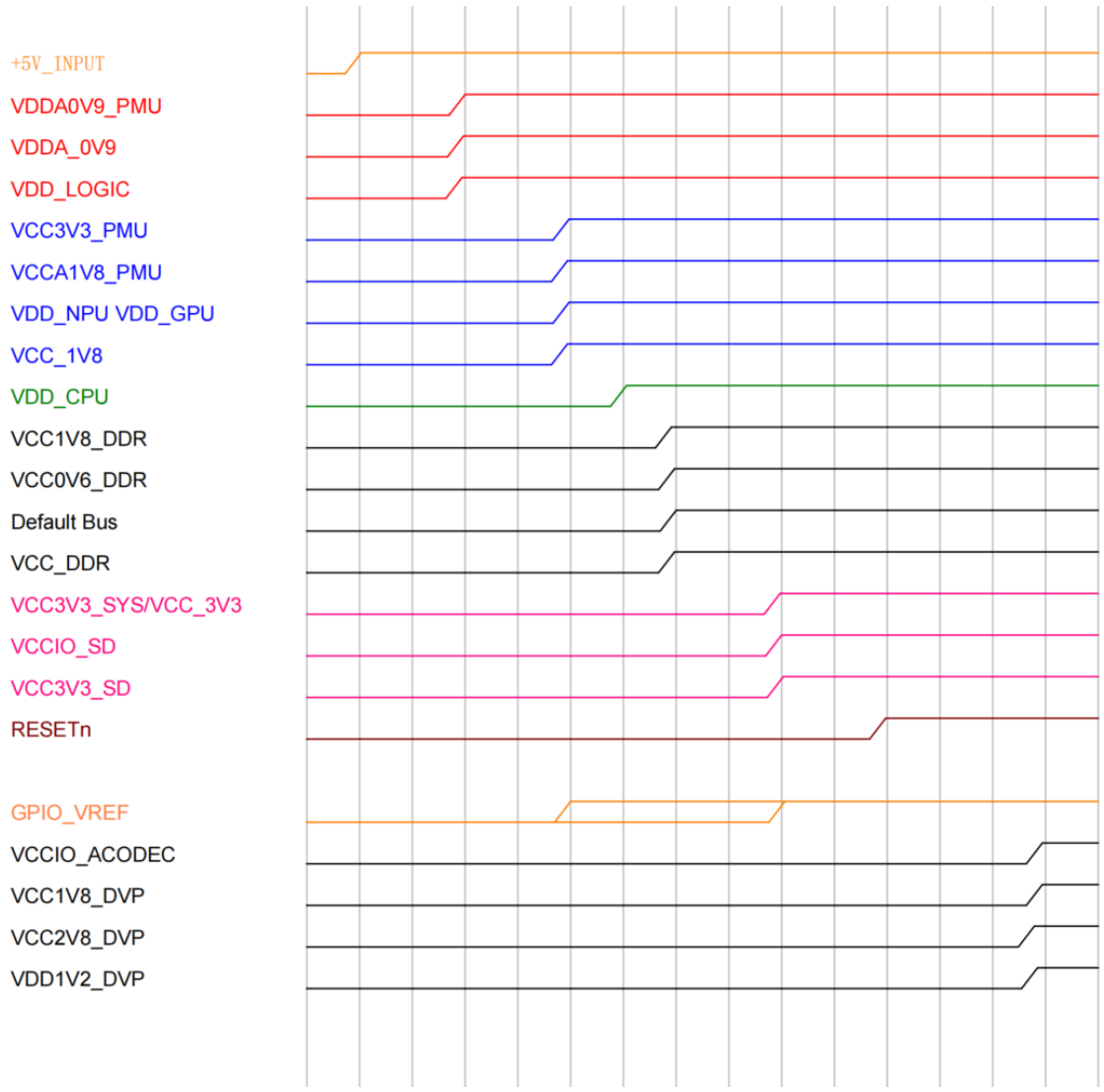

Figure 4: *Power On Sequence*

3.2 USB 2.0

3.2.1 USB OTG Interfaces

The CM3 module provides a set of USB 2.0 OTG interfaces that support both USB device and host modes. The USB_OTG0_ID pin is internally pulled up (approximately 200KOhm) to USB_AVDD_1V8. By default, the OTG interface operates in device mode. When an OTG device is connected, the USB_OTG0_ID pin is pulled low, indicating a switch to host mode. The USB_OTG0_VBUSDET pin is connected to a voltage divider circuit to detect the pres-

ence of a USB device. A high voltage level (2.7V-3.3V) indicates the presence of a USB connection. It is recommended to connect this pin regardless of using the OTG port or for programming purposes. To suppress electromagnetic radiation, it is advised to include a common-mode inductor in the signal line. Additionally, for improved interface robustness, a 2.2 Ohm resistor should be connected in series, and ESD protection measures should be implemented. The parasitic capacitance of the ESD protection device should be less than 1pF, and it should be placed close to the USB interface. Refer to the following diagram for more details.

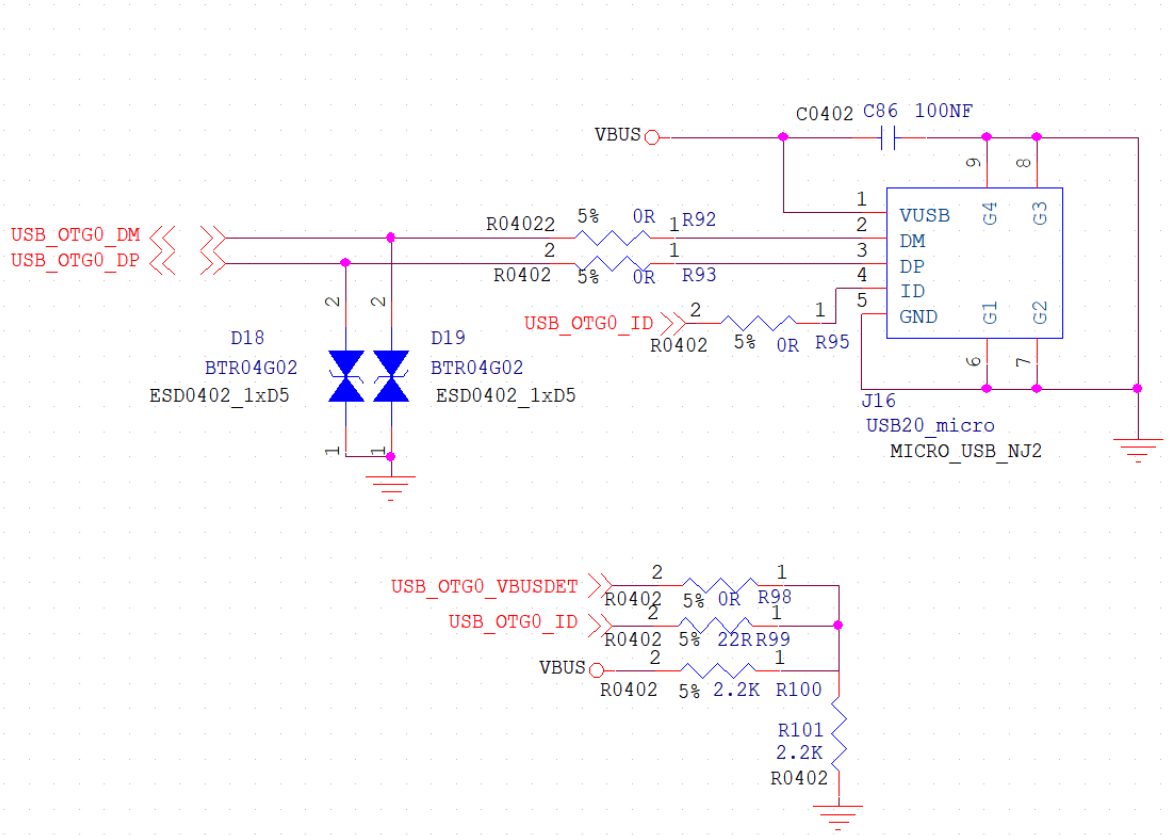

Figure 5: *USB OTG Reference Design*

`USB_OTG0_VBUSDET` must be connected. `USB_OTG0_VBUSDET` is signal high valid at a voltage range of 2.7-3.3V, typically 3.0V.

3.2.2 USB HOST Interfaces

The CM3 module provides three sets of USB 2.0 HOST interfaces. These interfaces allow the module to act as a host for USB devices such as peripherals, storage devices, and input devices. The protection design for the USB 2.0 HOST interfaces can be referenced from the USB 2.0 OTG interface. Please consult the respective schematics for detailed information.

The CM3 module also includes one set of USB 3.0 HOST interfaces. When utilizing the full functionality of USB 3.0 HOST, one set of USB 2.0 HOST interfaces will be occupied, leaving two sets available for USB 2.0 HOST usage.

Please refer to the CM3 datasheet for comprehensive technical information regarding the USB interfaces and their respective pin configurations.

Radxa CM3 provides two USB HOST and one USB OTG interfaces, which comply with USB 2.0 high speed (480 Mbps) and full speed (12 Mbps). `USB_OTG0` can be used for firmware upgrades. If the final product does not utilize this function, it is highly recommended to reserve it for debugging or production purposes. Leave `USB_OTG0_ID` not connected if it is not used.

The trace lengths of the USB 2.0 signals on the compute module are as follows:

Signal	Length
`USB2_HOST2_DM`	2428.412mil
`USB2_HOST2_DP`	2384.503mil
`USB2_HOST3_DM`	2212.094mil
`USB2_HOST3_DP`	2178.789mil
`USB_OTG0_DM`	740.447mil
`USB_OTG0_DP`	732.221mil

3.3 MMC/SD Card

The SDMMC0 interface on Radxa CM3 supports SD V3.01 and MMC V4.51 specifications. It can be used for an OS boot SD card or as data storage.

`VCCIO_SD` (PIN92) is the IO interface power supply for the SDMMC0 controller, providing 3.3V power (SD V2.0 mode) or adjustable 3.3V/1.8V power (SD V3.0 mode). The SDMMC0

signal lines already have internal pull-up resistors and do not require additional external pull-ups. On the CM3 compute module, a series resistor of 22ohm is placed near the chip end of SDMMC0_CLK. If users need to design a baseboard, please refer to the schematic diagram below:

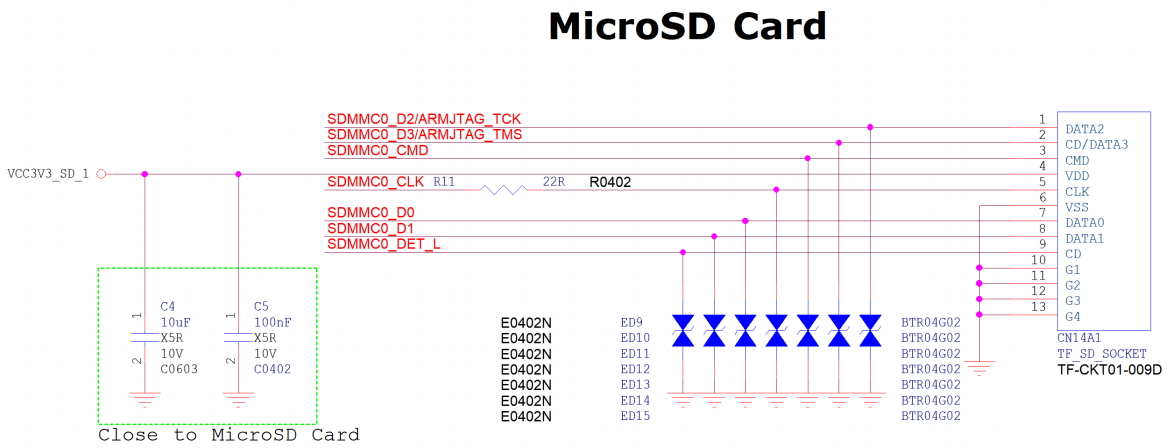

Figure 6: *SD Card Reference Design*

- SDMMC0 is multiplexed with JTAG and other functions, and the function is selected through SDMMC0_DET. Refer to the JTAG section for details.
- ESD devices should be placed near the SD card slot for signals. To minimize the impact on the signal, it is recommended to select a model with a junction capacitance of less than 1pF (if only SD2.0 mode is required, the junction capacitance of the ESD device can be relaxed to less than 9pF).

Signal	Pull-Up/Down	Connection	Resistance	Description
SDMMC0_DQ[3]	Pull-Up	Series 22ohm Resistor	22ohm	SD Data Transmit/Receive
SDMMC0_DQ[2]	Pull-Up	Series 22ohm Resistor	22ohm	SD Data Transmit/Receive
SDMMC0_DQ[1]	Pull-Up	Series 22ohm Resistor	22ohm	SD Data Transmit/Receive
SDMMC0_DQ[0]	Pull-Up	Series 22ohm Resistor	22ohm	SD Data Transmit/Receive
SDMMC0_CLK	Pull-Down	Series 22ohm Resistor	22ohm	Placed near RK3566, SD Clock Transmit
SDMMC0_CMD	Pull-Up	Series 22ohm Resistor	22ohm	SD Command Transmit/Receive
SDMMC0_DET	Pull-Up	Series 100ohm Resistor	100ohm	SD Card Insertion Detection

The above information is for SDMMC0. The other two SDMMC interfaces have similar specifications and requirements.

SDIO Layout Requirements

Parameter	Requirement
Trace Impedance	50Ω ±10% single ended
Data to clock mismatch	<120mil
Max trace length (data rate ≤50Mbps)	<6 inches
Max trace length (data rate >50Mbps)	<4 inches
Minimum spacing of SDIO Signals	At least 2 times the width of SDIO trace
Maximum allowed via	Recommend ≤4 vias

The trace length of the SDIO signal on the compute module.

Signal	Length
SDMMC0_CLK	1645.516mil
SDMMC0_CMD	1368.932mil
SDMMC0_D0	1477.469mil
SDMMC0_D1	1413.775mil
SDMMC0_D2	1493.113mil
SDMMC0_D3	1377.778mil

3.4 Gigabit Ethernet

The RADXA CM3 board integrates a Gigabit PHY chip, RTL8211F. Four sets of differential signals, PHY1_MDI0, PHY1_MDI01, PHY1_MDI02, and PHY1_MDI03, are connected to the B2B connector. When operating at 1000BASE-T, all four sets of differential signals are used. When operating at 100BASE-TX, only PHY1_MDI0 and PHY1_MDI01 are utilized.

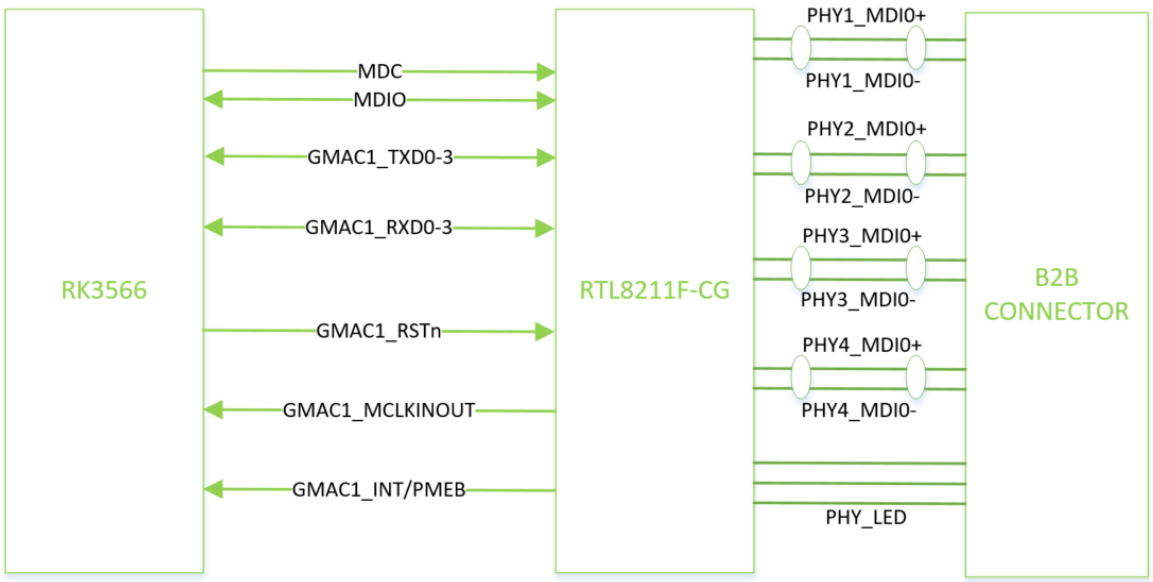

Figure 7: *PHY Design*

The RTL8211F is a voltage mode PHY, and when using it, the center tap of the transformer should be connected to ground through a 1uF capacitor.

On the CM3 compute module, four series common-mode inductors are placed in line with the four sets of differential signals. These inductors help suppress electromagnetic interference (EMI) and provide common-mode filtering. When designing a custom baseboard, refer to the provided design as follows:

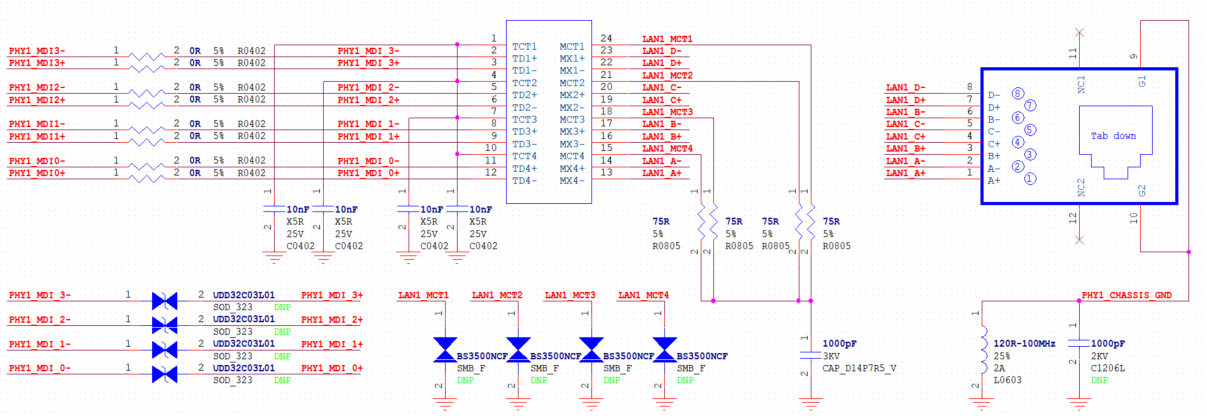

Figure 8: *Ethernet Reference Design*

The trace length of the MDI signal on the compute module.

Signal	Length
PHY1_MDI0+	319.903mil
PHY1_MDI0-	326.000mil
PHY1_MDI1+	249.671mil
PHY1_MDI1-	277.370mil
PHY1_MDI2+	394.321mil
PHY1_MDI2-	400.440mil
PHY1_MDI3+	335.779mil
PHY1_MDI3-	347.346mil

The differential signals of the MDI (Medium Dependent Interface) for Gigabit Ethernet generally control the differential impedance at 100 ohms.

3.5 Display

3.5.1 HDMI

HDMI (High-Definition Multimedia Interface) is a unified method of transferring video and audio data over a TMDS (Transition Minimized Differential Signaling) compatible physical link to an audio/visual display device. The HDMI interface is electrically compatible with the DVI (Digital Visual Interface) standard.

Features:

- HPD (Hot Plug Detect) input analog comparator
- Input reference clock range of 13.5–600MHz
- Support for up to 10 bits Deep Color modes
- Aggregate bandwidth of up to 18Gbps
- Support for video resolutions up to 1080p@120Hz and 4096x2304@60Hz
- Compatibility with 3-D video formats

Signal	Impedance	Description
HDMI_TX_DP/DN[2:0]	100ohm±10%	HDMI TX data transmission
HDMI_TX_CLKP/CLKN	100ohm±10%	HDMI TX clock transmission
HDMI_TX_HPDIN	Not specified	HDMI TX hot-plug detection

Signal	Impedance	Description
HDMI_TX_REXT	Not specified	External resistor for HDMI reference connection(Default: 1% precision 1.62k resistor)
HDMITX_SCL/SDA	Not specified	HDMI data communication channel
HDMITX_CEC	Not specified	HDMI Consumer Electronics Control pin

On the RADXA CM3 compute module, the HDMITX_SCL/SDA and HDMITX_CEC signals have already been processed through level translation. The HDMI_TX_HPDIN signal has a 100k ohm pull-down resistor and is series-connected to the RK3566 through a 1k ohm resistor. When designing a baseboard, users don't need to worry about the level translation issue. Please refer to the following design:

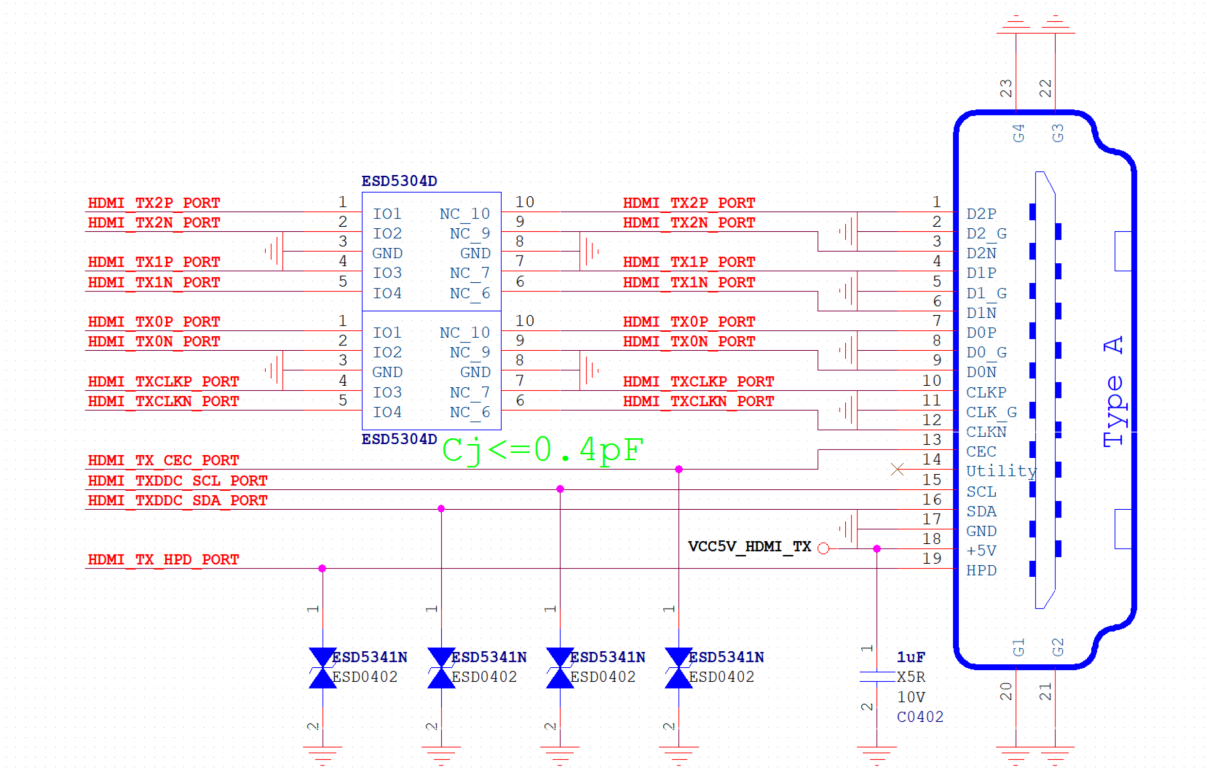

Figure 9: *HDMI Reference Design*

HDMI 2.0 Layout Requirements

Parameter	Requirement
Trace Impedance	100Ω ±10% differential
Max intra-pair skew	<12mil
Max mismatch between clock and data pairs	<480mil
Max trace length on carrier board	<6 inches

Parameter	Requirement
Minimum pair to pair spacing	≥5 times the width of HDMI trace (At least 4 times the width of HDMI trace)
Minimum spacing between HDMI and other Signals	≥5 times the width of HDMI trace (At least 4 times the width of HDMI trace)
Maximum allowed via	Recommend ≤ 2 vias

The trace length of the HDMI signal on the compute module.

Signal	Signal
HDMI_TX0N_PORT	1310.556mil
HDMI_TX0P_PORT	1302.62mil
HDMI_TX1N_PORT	1218.286mil
HDMI_TX1P_PORT	1156.647mil
HDMI_TX2N_PORT	1122.794mil
HDMI_TX2P_PORT	1118.675mil
HDMI_TXCLKN_PORT	1437.63mil
HDMI_TXCLKP_PORT	1,398.265mil

3.5.2 eDP

The RK3566 integrates an eDP (Embedded DisplayPort) v1.3 controller, which supports data rates of 1.62Gbps/lane and 2.7Gbps/lane. It can operate in 1-lane, 2-lane, and 4-lane modes, with a maximum output resolution of 2560x1600@60Hz. The eDP interface also includes an AUX channel with a maximum rate of 1Mbps.

For the coupled differential signals in the eDP interface, it is recommended to place 100nF coupling capacitors near the transmitter side. It is suggested to use 0201 package size capacitors to reduce ESR (Equivalent Series Resistance) and ESL (Equivalent Series Inductance).

eDP interface features:

- Supports 1 eDP 1.3 interface
- Supports up to 4 physical lanes of 2.7Gbps
- Supports Panel Self Refresh (PSR)

- Supports resolutions up to 2560x1600@60Hz
- Supports RGB format with up to 10 bits

The impedance and description of the eDP interface signals are as follows:

Signal	Impedance	Description
eDP_TX_DP/DN[3:0]	100ohm±10%	eDP TX data transmission, coupled with 100nF capacitor
eDP_TX_AUXP/N	100ohm±10%	eDP TX auxiliary channel, coupled with 100nF capacitor
eDP_HPDIN	N/A	No eDP TX insertion detection

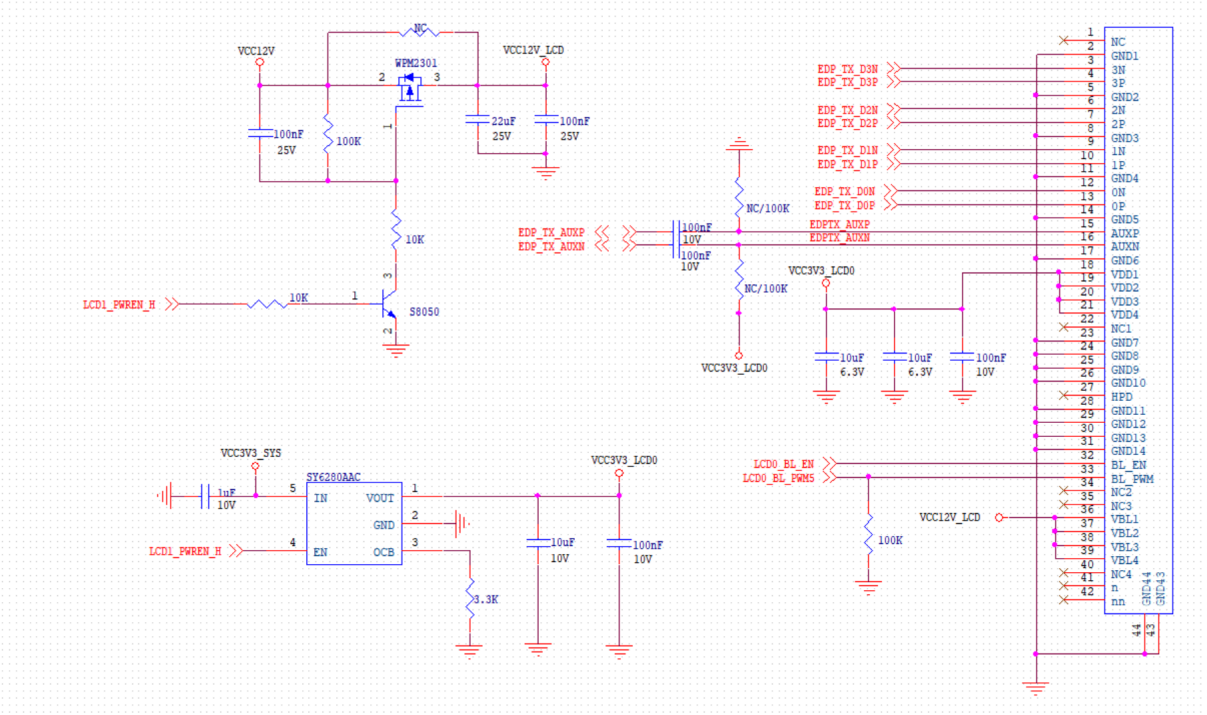

Figure 10: *EDP Reference Design*

eDP Layout Requirements

Parameter	Requirement
Trace Impedance	100Ω ±10% differential
Max intra-pair skew	<12mil
Max trace length on carrier board	<6 inches
Minimum pair to pair spacing	Recommend ≥4 times the width of eDP trace
AC coupling capacitors	100nF ±20%, discrete 0201 package preferable
Minimum spacing between eDP and other signals	≥4 times the width of eDP trace
Maximum allowed via	Recommend ≤ 4 vias

The trace length of the eDP signals on the compute module.

Signal	Length
EDP_TX_AUXN	1125.784mil
EDP_TX_AUXP	1145.200mil
EDP_TX_D0N	1,551.442mil
EDP_TX_D0P	1,605.627mil
EDP_TX_D1N	1,394.502mil
EDP_TX_D1P	1,387.683mil
EDP_TX_D2N	1,223.146mil
EDP_TX_D2P	1,278.783mil
EDP_TX_D3N	1,074.909mil
EDP_TX_D3P	1,092.072mil

At the connector end of the eDP display, it is recommended to have a 100k pull-down resistor reserved for AUXP and a 100k pull-up resistor reserved for AUXN.

3.5.3 MIPI CSI

The RK3566 processor includes a built-in ISP (Image Signal Processor) that supports two sets of MIPI-CSI (Mobile Industry Processor Interface - Camera Serial Interface) inputs. Each set consists of 4 lanes, compliant with the MIPI V1.2 standard, and has two sets of clocks. The MIPI-CSI interface supports both 2-lane and 4-lane input modes.

In 4-lane mode, the `MIPI_CSI_RX_D[3:0]` data signals are synchronized with the CLK0 clock. In 2-lane mode, two cameras can be supported. The `MIPI_CSI_RX_D[1:0]` data signals are synchronized with the CLK0 clock, and the `MIPI_CSI_RX_D[3:2]` data signals are synchronized with the CLK1 clock. The MCLK (Master Clock) for the camera can be obtained from the following clock outputs of the RK3566: `CAM_CLKOUT0`, `CAM_CLKOUT1`, `CIF_CLKOUT`, and `REFCLK_OUT`. Ensure that the corresponding IO levels are compatible with the camera's IO levels.

When using two cameras, it is important to determine whether to power the cameras separately or together. Additionally, the I2C addresses of the cameras should be checked for any differences. If the addresses are the same, the cameras should be connected to two independent I2C controllers.

The impedance and description of the MIPI-CSI interface signals are as follows:

Signal	Impedance	Description
MIPI_CSI_RX_DP/DN[3:0]	100ohm±10%	MIPI CSI0 data reception
MIPI_CSI_RX_CLK0P/N	100ohm±10%	MIPI 4-lane mode clock or 2-lane mode CLK0
MIPI_CSI_RX_CLK1P/N	100ohm±10%	MIPI 2-lane mode CLK1

MIPI Layout Requirements

Parameter	Requirement
Trace Impedance	100Ω ±10% differential
Max intra-pair skew	<12mil
Data to clock mismatch	<36mil
Max trace length	<6 inches
Maximum allowed via	4
Minimum pair to pair spacing	Recommend ≥3 times the width of MIPI trace (Try to increase spacing between pairs whenever possible)
Minimum spacing between MIPI and other Signals	Recommend ≥3 times the width of MIPI trace

The lengths of MIPI-CSI signal routing on the compute module are as follows:

Signal	Length
MIPI_CSI_RX_CLK0N	1400.512mil
MIPI_CSI_RX_CLK0P	1395.610mil
MIPI_CSI_RX_CLK1N	2670.288mil
MIPI_CSI_RX_CLK1P	2603.709mil
MIPI_CSI_RX_D0N	2412.854mil
MIPI_CSI_RX_D0P	2394.800mil
MIPI_CSI_RX_D1N	1411.662mil
MIPI_CSI_RX_D1P	1371.762mil
MIPI_CSI_RX_D2N	1561.542mil
MIPI_CSI_RX_D2P	1565.460mil
MIPI_CSI_RX_D3N	2546.373mil
MIPI_CSI_RX_D3P	2497.610mil

3.5.4 MIPI DSI0 / LVDS

The RK3566 processor integrates two MIPI-DSI (Mobile Industry Processor Interface - Display Serial Interface) controllers, both of which are 4-lane interfaces capable of operating at speeds up to 2.5Gbps per lane. The maximum output resolution supported is 1920x1080@60Hz.

For users designing their own boards with MIPI-DSI, it is important to consider proper equal-length design of the MIPI signals. This can be achieved by controlling the total wiring length between the compute module and the baseboard. The specifications provided in the MIPI-CSI chapter are applicable to MIPI-DSI and should be referred to accordingly. To determine the wiring length of the MIPI-DSI signals on the compute module, please refer to the table below.

Key features of the MIPI DSI0 interface:

- Compatible with MIPI Alliance Interface specification v1.2
- Supports 2 channels of DSI
- Supports 4 data lanes per channel
- Supports a maximum data rate of 2.5Gbps per lane
- Supports display output resolutions of up to 1920x1080@60Hz in single MIPI mode and 2560x1440@60Hz in dual-MIPI mode
- Supports RGB format with up to 8 bits

The impedance and description of the MIPI-DSI interface signals are as follows:

Signal	Impedance	Description
MIPI_DSI_TX0_DP/DN[3:0]	100ohm±10%	MIPI DSI0 data transmission
MIPI_DSI_TX0_CLKP/CLKN	100ohm±10%	MIPI DSI0 clock transmission
MIPI_DSI_TX1_DP/DN[3:0]	100ohm±10%	MIPI DSI1 data transmission
MIPI_DSI_TX1_CLKP/CLKN	100ohm±10%	MIPI DSI1 clock transmission

The MIPI-DSI0 interface mentioned above also shares a set of LVDS (Low-Voltage Differential Signaling) signals. The RK3566 processor integrates an LVDS controller that supports a maximum output resolution of 1280x800@60Hz. To switch to the corresponding functionality, software configuration is required.

The impedance and description of the LVDS interface signals are as follows:

Signal	Impedance	Description
LVDS_TX0_DP/DN[3:0]	100ohm±10%	LVDS TX0 data transmission differential signals

Signal	Impedance	Description
LVDS_TX0_CLKP/CLKN	100ohm±10%	LVDS TX0 clock transmission differential signals

The lengths of the MIPI-DSI signal routing on the compute module are provided in the following table:

Signal	Length
MIPI_DSI_TX0_CLKN/LVDS_TX0_CLKN	1033.672mil
MIPI_DSI_TX0_CLKP/LVDS_TX0_CLKP	1079.098mil
MIPI_DSI_TX0_D0N/LVDS_TX0_D0N	853.225mil
MIPI_DSI_TX0_D0P/LVDS_TX0_D0P	855.822mil
MIPI_DSI_TX0_D1N/LVDS_TX0_D1N	907.347mil
MIPI_DSI_TX0_D1P/LVDS_TX0_D1P	944.418mil
MIPI_DSI_TX0_D2N/LVDS_TX0_D2N	793.258mil
MIPI_DSI_TX0_D2P/LVDS_TX0_D2P	817.433mil
MIPI_DSI_TX0_D3N/LVDS_TX0_D3N	787.867mil
MIPI_DSI_TX0_D3P/LVDS_TX0_D3P	747.476mil

3.5.5 MIPI DSI 1

The compute module provides the following table indicating the lengths of MIPI_DSI1 signal routing:

Signal	Length
MIPI_DSI_TX1_CLKN	1088.401mil
MIPI_DSI_TX1_CLKP	1078.066mil
MIPI_DSI_TX1_D0N	1007.536mil
MIPI_DSI_TX1_D0P	1084.659mil
MIPI_DSI_TX1_D1N	1340.710mil
MIPI_DSI_TX1_D1P	1311.399mil

Signal	Length
MIPI_DSI_TX1_D2N	1198.503mil
MIPI_DSI_TX1_D2P	1188.801mil
MIPI_DSI_TX1_D3N	1658.945mil
MIPI_DSI_TX1_D3P	1581.330mil

3.6 USB3, PCI Express, and SATA

The RK3566 SoC's Multi-PHY Interface supports multiple high-speed interfaces, including PCIe2.1, SATA3.0, and USB3.0. Here are some key points about the Multi-PHY Interface:

- It supports three multi-PHYs, each capable of PCIe2.1/SATA3.0/USB3.0.
- It can accommodate up to one USB3.0 Host controller.
- It can accommodate up to one PCIe2.1 controller.
- It can accommodate up to two SATA controllers.
- Multi-PHY1 can support either a USB3.0 Host or SATA1 interface.
- Multi-PHY2 can support either a PCIe2.1 or SATA2 interface.

USB 3.0 xHCI Host Controller:

- It supports 1 USB2.0 port and 1 Super-Speed port.
- It allows concurrent USB3.0/USB2.0 traffic with a bandwidth of up to 8.48Gbps.
- It supports standard or open-source xHCI and class drivers.

PCIe2.1 interface:

- It is compatible with the PCI Express Base Specification Revision 3.0.
- It supports Root Complex (RC) mode.
- It supports a serial data transmission rate of 2.5Gbps or 5.0Gbps per lane per direction.
- It supports one lane.

SATA interface:

- It is compatible with Serial ATA 3.3 and AHCI Revision 1.3.1.
- It supports eSATA.
- It supports data transmission rates of 1.5Gb/s, 3.0Gb/s, and 6.0Gb/s.
- It supports three SATA controllers.

The table below shows the supported interface configurations for the Multi-PHYs:

Scenario	PHY 1	PHY 2
1	USB3.0	PCIE2.0
2	USB3.0	SATA3.0_2
3	SATA3.0_1	PCIE2.0
4	SATA3.0_1	SATA3.0_2

3.6.1 PCIE2.0

The following specifications and layout requirements should be considered when designing PCIe 2.0:

- Pay attention to the power supply requirements of PCIe peripherals, especially when designing slots. External devices should be fully considered.
- For PCIe TX/RX differential signal interconnection, use 0201 package for the 100nF AC coupling capacitor to reduce ESR and ESL and minimize impedance discontinuity.
- `PCIE20_CLKREQn` and `PCIE20_WAKEn` must use specific functional pins and cannot be replaced by other IOs. They must also be in the same MUX group, indicated by the same `_Mx` suffix.
- `PCIE20_PERSTn` can be replaced by functional pins or GPIO. When choosing functional pins, ensure they are in the same MUX group as PCIE20_CLKREQn and PCIE20_WAKEn (with the same `_Mx` suffix).
- For a standard PCIe slot, `PCIE20_PERSTn`, `PCIE20_CLKREQn`, and `PCIE20_WAKEn` all operate at a 3.3V voltage level.
- `PCIE20_PRSNT` is the insert detection pin for Add In Cards and can be implemented using GPIO.

The table below provides the lengths of PCIE2.0 signal routing on the compute module:

Signal	Length
`PCIE20_REFCLKN`	934.064mil
`PCIE20_REFCLKP`	947.955mil
`PCIE20_RXN`	899.466mil

Signal	Length
PCIE20_RXP	930.440mil
PCIE20_TXN	835.025mil
PCIE20_TXP	823.365mil

3.6.2 SATA 3.0

SATA (Serial Advanced Technology Attachment) is a serial communication hard disk interface supported by RK3566. It adheres to the SATA V3.0 protocol and offers the following features:

- Compatibility with Gen1 / Gen2 / Gen3 standards.
- Support for a maximum signal transmission rate of 6GT/s on a single data channel.
- Support for Out-of-Band (OOB) communication.
- Support for SATA Power Management (PM) function and connection with external expansion chips.
- Support for spread spectrum function.

The table below provides the impedance and description of the SATA interface signals:

Signal	Impedance	Description
SATAx_TXP/N	90ohm±10%	SATA data send, place the coupling capacitor 10nF close to the mainboard connector
SATAx_RXP/N	90ohm±10%	SATA data receive, place the coupling capacitor 10nF close to the mainboard connector

The following layout requirements should be considered for SATA 3.0:

Parameter	Requirement
Trace Impedance	100Ω ±10% differential
Max intra-pair skew	<12mil
Max trace length on carrier board	<6 inches
AC coupling capacitors	10nF ±20%, discrete 0201 package preferable
Minimum pair-to-pair spacing	≥4 times the width of SATA trace
Minimum spacing between SATA and other signals	≥4 times the width of SATA trace
Maximum allowed via	Recommend ≤ 2 vias

3.6.3 USB 3.0

The RK3566 chip features one USB2.0 OTG port, three USB2.0 HOST ports, and one USB3.0 HOST port (one USB2.0 host will be occupied when using the full USB3.0 HOST).

The following layout requirements should be considered for USB 3.0:

Parameter	Requirement
Trace Impedance	90Ω ±10% differential
Max intra-pair skew	<12mil
Max trace length on carrier board	<6 inches
AC coupling capacitors	100nF ±20%, discrete 0201 package preferable
Minimum pair-to-pair spacing	≥4 times the width of USB trace
Minimum spacing between USB and other signals	≥4 times the width of USB trace
Maximum allowed via	Recommend ≤ 2 vias

The table below provides the lengths of USB3.0 signal routing on the compute module:

Signal	Length
USB3_HOST1_DM	889.544mil
USB3_HOST1_DP	873.591mil
USB3_HOST1_SSRXN	848.957mil
USB3_HOST1_SSRXP	815.919mil
USB3_HOST1_SSTXN	818.027mil
USB3_HOST1_SSTXP	844.455mil

3.7 GPIO

To ensure proper operation and prevent potential risks, follow the guidelines below for configuring GPIO in relation to hardware and software voltage levels:

1. Match Software Configuration to Hardware IO Level:
    - When the hardware IO level is connected to 1.8V, configure the software voltage to 1.8V.
    - When the hardware IO level is connected to 3.3V, configure the software voltage to 3.3V.
2. VCCIO2 Power Domain:
    - The VCCIO2 power domain does not require software configuration. However, the hardware power supply voltage must match the status of the FLASH_VOL_SEL pin:

  - When the VCCIO2 power supply is 1.8V, the FLASH_VOL_SEL pin must remain at a high level.
  - When the VCCIO2 power supply is 3.3V, the FLASH_VOL_SEL pin must be kept at a low level.

Failure to adhere to these guidelines may result in the following risks:

- Software configured to 1.8V while hardware power supply is 3.3V can lead to IO being in an overvoltage state, potentially causing long-term damage to the IO.
- Software configured to 3.3V while hardware power supply is 1.8V may result in abnormal IO functionality.

If there are changes to the power domain in the customer project, it is essential to update the voltage configurations accordingly to ensure proper operation.

3.8 Wi-Fi and Bluetooth Connectivity

The RK3566 chip incorporates Wi-Fi and Bluetooth capabilities through the following interfaces and features:

3.8.1 Wi-Fi (SDIO Interface)

The SDMMC1 interface of the RK3566 is utilized as an SDIO interface to connect with the Wi-Fi module. Key details include:

- Operating voltage: 1.8V
- Supports SDIO 3.0 high-speed mode

3.8.2 Bluetooth (UART1 Interface and I2S Interface)

The CM256 module facilitates Bluetooth audio functionality and is connected to the RK3566 chip via the following interfaces:

- UART1 Interface: Four-wire UART interface used for Bluetooth communication.
- I2S Interface: Additional I2S interface available between the SoC and the Wi-Fi module specifically for Bluetooth audio. It uses the i2s2 instance of the SoC.

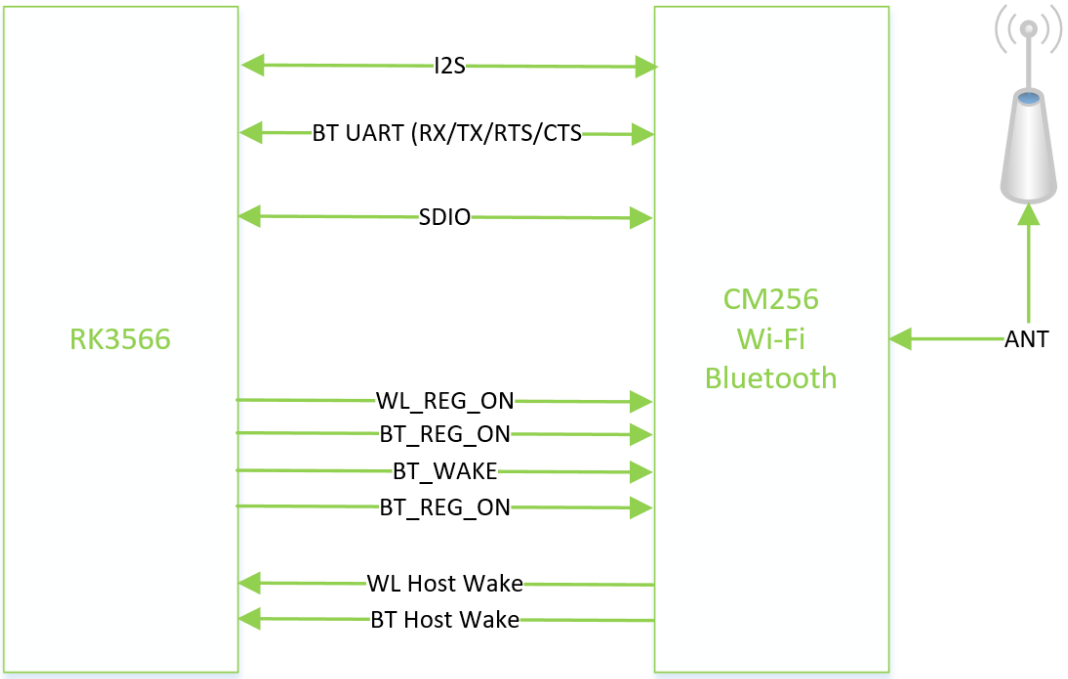

Figure 11: *Wi-Fi and Bluetooth Block Diagram*

3.8.3 WLAN Features

The Wi-Fi module offers the following features:

- High-speed wireless connection with a transmit/receive PHY rate of up to 433.3Mbps using 80MHz bandwidth.
- Utilizes one antenna to support 1 transmit and 1 receive technology, as well as Bluetooth functionality.
- Wireless Coexistence System (WCS) for optimized performance in coexistence scenarios.
- Low power consumption while maintaining high performance.
- Enhanced wireless security for secure connections.
- Supports Piconet and Scatternet configurations for flexible network setups.
- Compact form factor with dimensions of 12mm (L) x 12mm (W) x 1.65mm (H) in an LGA package.

- Dual-band operation supporting 2.4 GHz and 5GHz frequencies compliant with 802.11 a/b/g/n/ac standards.
- Requires an external crystal for operation.

3.8.4 Bluetooth Features

The Bluetooth module provides the following features:

- Utilizes one antenna to support 1 transmit and 1 receive technology, as well as Bluetooth functionality.
- Fully qualified Bluetooth BT4.2 compliant.
- Compliant with BT5.0 standards.
- Supports Enhanced Data Rate (EDR) compliant for both 2Mbps and 3Mbps data rates.
- Offers high-speed UART and PCM interfaces for Bluetooth communication.

These Wi-Fi and Bluetooth capabilities enhance the connectivity options of the Radxa CM3, enabling wireless communication and audio functionality in various applications.

3.8.5 Antenna Connection

The Radxa CM3 wireless module does not come with any pre-connected antennas. It requires appropriate antennas for wireless and Bluetooth functionality. Depending on the enclosure design, you can choose to use internal or external antennas. The location of the antenna connection on the top side of the board is indicated as item ⑤ in Figure 2.

The wireless module utilizes a standard 2x2 mm RF micro coaxial receptacle (connector) with an outer diameter of 1.5 mm. When selecting the appropriate plug, ensure it is compatible with the cable diameter. Refer to the figure below for the minimum requirements and dimensions of the compatible RF connectors and mating plugs.

- Receptacle physical outline: 2mm x 2mm x 0.6mm
- Receptacle outer diameter: 1.5mm

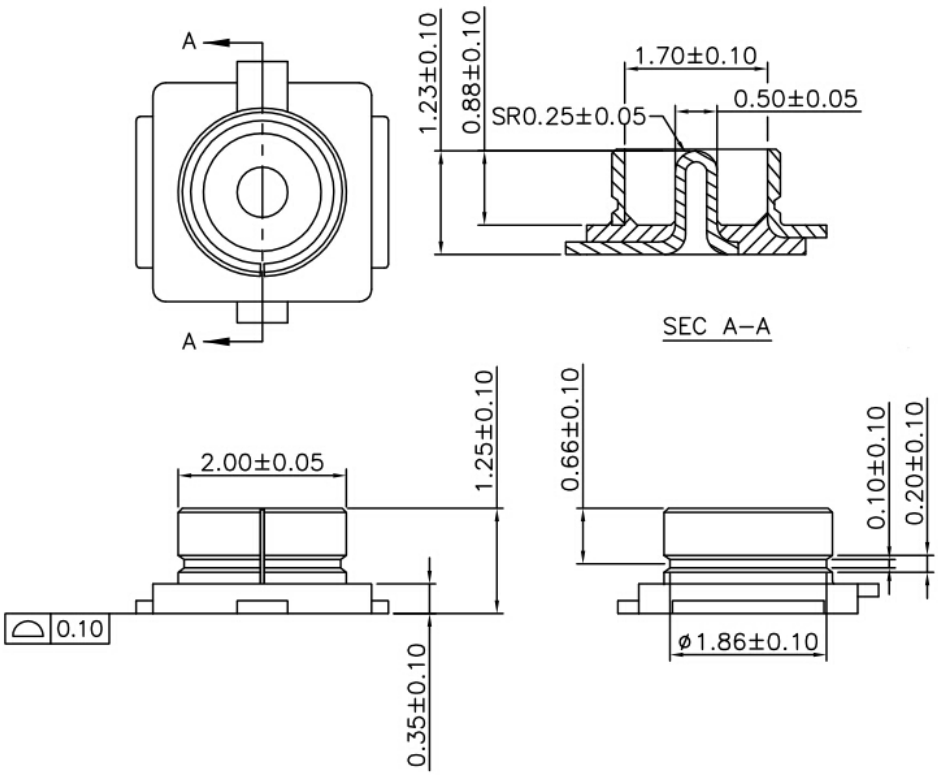

Figure 12: *Radxa CM3 Antenna Dimensions*

Note:
The specific antenna requirements and selection may vary based on your application and desired wireless performance.

3.9 I2C

The RADXA CM3 compute module provides seven sets of I2C interface s for the baseboard. Here are the details of each interface:

1. **I2C2_SDA_M1** and **I2C2_SCL_M1**:
    - Power domain: `GPIO_VREF` (provided by the baseboard)
    - Voltage options: 1.8V or 3.3V
    - Pull-ups: Users need to add pull-ups on the baseboard if the y choose to use these interfaces.

2. **I2C4_SCL_M0** and **I2C4_SDA_M0**:
    - Power domain: `GPIO_VREF` (provided by the baseboard)
    - Voltage options: 1.8V or 3.3V
    - Pull-ups: Users need to add pull-ups on the baseboard if they choose to use these interfaces.
3. **I2C2_SCL_MO** and **I2C2_SDA_MO**:
    - Power domain: 1.8V
    - Pull-ups: Pull-ups are already present on the mainboard, so users do not need to add pull-ups on the baseboard if they choose to use these interfaces.
4. **HDMITX_SDA** and **HDMITX_SCL**:
    - Power domain: 5V
    - Pull-ups: Users need to add pull-ups on the baseboard if they want to use this interface. Compute module does not have pull-ups for this interface.
5. **I2C3_SDA_M0** and **I2C3_SCL_M0**:
    - Power domain: `VCCIO_ACODEC`
    - Voltage options: 1.8V or 3.3V (configurable from the PMIC)
    - Pull-ups: Pull-ups are already present on the compute module, so users do not need to add pull-ups on the baseboard.
6. **I2C1_SDA** and **I2C1_SCL**:
    - Power domain: 1.8V
    - Pull-ups: Users need to add 1.8V pull-ups on the baseboard if they choose to use these interfaces. Compute module does not have pull-ups for this interface.

The following table provides a summary of the I2C interfaces on the compute module:

Pin Number	Compute Module Symbol	RK3566	Power Domain	Compute Module Pull-up
J69_36	I2C2_SDA_M1	I2C2_SDA_M1	GPIO_VREF (1V8_3.3V)	N (pull-up required)
J69_35	I2C2_SCL_M1	I2C2_SCL_M1	GPIO_VREF (1V8_3.3V)	N (pull-up required)
J69_38	SPI3_CLK_M0	I2C4_SCL_M0	GPIO_VREF (1V8_3.3V)	N (pull-up required)
J69_40	SPI3_MOSI_M0	I2C4_SDA_M0	GPIO_VREF (1V8_3.3V)	N (pull-up required)
J69_56	I2C2_SCL_MO	I2C2_SCL_MO	1.8V	Y (pull-up already present)
J69_58	I2C2_SDA_MO	I2C2_SDA_MO	1.8V	Y (pull-up already present)
J69_80	I2C0_SCL_PMIC	I2C0_SCL	1.8V	Y (pull-up already present)
J69_82	I2C0_SDA_PMIC	I2C0_SDA	1.8V	Y (pull-up already present)
J68_199	HDMI_TXDDC_SDA_PORT	HDMITX_SDA	5V	N (pull-up required)
J68_200	HDMI_TXDDC_SCL_PORT	HDMITX_SCL	5V	N (pull-up required)
J1_44	I2C3_SCL_ACODEC	I2C3_SDA_M0	VCCIO_ACODEC	Y (pull-up already present)
J1_46	I2C3_SDA_ACODEC	I2C3_SCL_M0	VCCIO_ACODEC	Y (pull-up already present)

Pin Number	Compute Module Symbol	RK3566	Power Domain	Compute Module Pull-up
J1_89	GPIO_B4	I2C1_SDA	1.8V	N (pull-up required)
J1_87	GPIO_B3	I2C1_SCL	1.8V	N (pull-up required)

Note: The table assumes that "Y" indicates the presence of a pull-up on the compute module, and "N" indicates the absence of a pull-up.

3.9.1 I2C Interface Features

- Supports both 7-bit and 10-bit address modes.
- Programmable clock frequency through software.
- Data transfer rates:
  - Standard mode: Up to 100Kbit/s.
  - Fast-mode: Up to 400Kbit/s.
  - Fast-mode Plus: Up to 1 Mbit/s.

These I2C interfaces provide flexible and versatile communication options for the Radxa CM3, allowing users to connect and communicate with various devices and peripherals on the baseboard.

3.10 SPI Interface Configuration

The RK3566 chip supports four SPI controllers, and the RADXA CM3 compute module has connected three of them to the connector for user access. The available SPI interfaces on the module are SPI0, SPI1, and SPI3. Here are the pin mappings for each interface:

- **SPI0**:
  - Chip-Select (CS0): J69_28
  - Master Out Slave In (MOSI): J69_58
  - Master In Slave Out (MISO): J69_30
  - Clock (CLK): J69_56
- **SPI1**:
  - Chip-Select (CS0): J1_3
  - Master Out Slave In (MOSI): J1_8
  - Master In Slave Out (MISO): J1_10

  - Clock (CLK): J1_12
  - Additional Chip-Select (CS1): J1_24

- **SPI3**:

  - Chip-Select (CS0): J69_39
  - Master Out Slave In (MOSI): J69_44
  - Master In Slave Out (MISO): J69_40
  - Clock (CLK): J69_38
  - Additional Chip-Select (CS1): J69_29

3.10.1 SPI Interface Features

- Supports one chip-select output (CS0) and some interfaces support an additional chip-select output (CS1).
- Supports both serial-master and serial-slave modes, which are software-configurable.

When using SPI signals, it's important to consider the power domain of the interface signals. Ensure that the power domain of the device on the baseboard corresponds to the CM3 compute module.

3.11 UART Interface Configuration

The RADXA CM3 compute module provides multiple UART interfaces for serial communication. Here are the available UART functions and their corresponding pin mappings:

- **UART0**:

  - TX: J1_93
  - RTS (Request To Send): J1_95
  - CTS (Clear To Send): J69_50

- **UART1**:

  - TX: J1_75
  - RX: J1_77
  - RTS: J69_89
  - CTS: J69_97

- **UART2**:

  - TX: J69_55

  - RX: J69_51

- **UART3**:
  - TX: J1_44
  - RX: J1_46

- **UART4**:
  - RX: J1_40

- **UART5**:
  - TX: J1_10
  - RX: J1_12
  - RTS: J69_61
  - CTS: J69_69

- **UART6**:
  - RX: J69_67

- **UART7**:
  - TX: J1_83
  - RX: J1_85

- **UART8**:
  - RX: J1_24

- **UART9**:
  - TX: J1_34
  - RX: J1_36
  - TX: J69_21
  - RX: J69_91

3.11.1 UART Interface Features

The UART interfaces on the compute module offer the following features:

- Embedded two 64-byte FIFOs for separate transmit (TX) and receive (RX) operations.
- Support for 5-bit, 6-bit, 7-bit, and 8-bit serial data transmission or reception.
- Standard asynchronous communication bits such as start, stop, and parity.

- Support for different input clock frequencies for UART operation, enabling baud rates of up to 4 Mbps.
- Auto flow control mode supported for UART0, UART1, UART3, UART4, and UART5.

When utilizing these UART signals on the B2B connector, please consider the following:

- Some UART signal groups may have missing signals, while others can be used for 4-wire UART communication.
- Pay attention to the power domain of the interface IOs and ensure compatibility during usage.

The UART interfaces provide versatile serial communication capabilities, allowing users to transmit and receive data asynchronously with various configuration options.

3.12 I2S

I2S1 Digital Audio Interface

The I2S1 interface features independent 8-channel output and 8-channel input. To accommodate the asynchronous sampling rate requirements for audio recording and playback, it provides two sets of bit clock and frame clock (SCLKTX/LRCKTX, SCLKRX/LRCKRX) accordingly. It's important to note that if SDOx and SDIx are only associated with one group of bit/frame clock, the default common clock used is SCLKTX/LRCKTX.

The I2S1 interface supports both master and slave working modes, which can be configured via software. It also supports three types of I2S formats (normal, left-justified, right-justified) and four types of PCM formats (early, late1, late2, late3). The I2S1 pins are multiplexed in two different power domains: I2S1_M0 is multiplexed in VCCIO1, but it has multiplexing conflicts for three SDOx and SDIx signals; I2S1_M1 is multiplexed in VCCIO6, allowing all signals to be fully derived. Please note that I2S1_M0 and I2S1_M1 cannot be used simultaneously; only one of them can be used at a time. It's necessary to adjust the power supply of the corresponding power domain to match the IO level of the I2S peripheral.

In the case of using the PMIC power supply solution, I2S1_M0 is typically utilized as the audio communication interface for the PMIC integrated Codec. Therefore, the VCCIO power supply for this group can directly utilize the PMIC's VCCIO_ACODEC power supply.

The pull-up/down and matching design recommendations for the I2S1 interface are summarized in the following table:

Signal	Internal Pull	Connection Method	Description
I2S1_8CH_MCLK	Pull Down	Series Connect	I2S system clock output for slave
I2S1_8CH_SCLK_TX	Pull Down	Series Connect	I2S bit clock (TX, related to Audio Play)
I2S1_8CH_LRCK_TX	Pull Down	Series Connect	I2S frame clock for channel selection (TX, related to Audio Play)
I2S1_8CH_SDO0	Pull Down	Direct Connection	I2S serial data 0 output
I2S1_8CH_SDO1	Pull Down	Direct Connection	I2S serial data 1 output
I2S1_8CH_SDO2	Pull Down	Direct Connection	I2S serial data 2 output
I2S1_8CH_SDO3	Pull Down	Direct Connection	I2S serial data 3 output
I2S1_8CH_SCLK_RX	Pull Down	Series Connect	I2S bit clock (RX, related to Audio Record)
I2S1_8CH_LRCK_RX	Pull Down	Series Connect	I2S frame clock for channel selection (RX, related to Audio Record)
I2S1_8CH_SDI0	Pull Down	Direct Connection	I2S serial data 0 input
I2S1_8CH_SDI1	Pull Down	Direct Connection	I2S serial data 1 input
I2S1_8CH_SDI2	Pull Down	Direct Connection	I2S serial data 2 input
I2S1_8CH_SDI3	Pull Down	Direct Connection	I2S serial data 3 input

I2S2 Digital Audio Interface

The I2S2 interface comprises independent 2-channel output and 2-channel input. To support asynchronous sampling rates for playback and recording, it also provides two sets of bit clock and frame clock (SCLKTX/LRCKTX, SCLKRX/LRCKRX) accordingly. Similar to I2S1, if SDOx and SDIx are associated with only one group of bit/frame clock, the default common clock used is SCLKTX/LRCKTX.

The I2S2 interface supports both master and slave working modes, which can be configured via software. It also supports three types of I2S formats (normal, left-justified, right-justified) and four types of PCM formats (early, late1, late2, late3). The I2S2 pins are multiplexed in two different power domains: I2S2_M0 is multiplexed in VCCIO4, and I2S2_M1 is multiplexed in VCCIO6, allowing all signals to be fully derived. Similar to I2S1, I2S2_M0 and I2S2_M1 cannot be used simultaneously; only one of them can be used at a time. It's necessary to adjust the power supply of the corresponding power domain to match the IO level of the I2S peripheral.

In designs incorporating Bluetooth functionality, I2S2, by default, utilizes M0 multiplexing as the PCM function to connect with Bluetooth peripherals. In such designs, it's essential to verify the appropriate connection relationship between the interface and the receiving/sending signals of the Bluetooth peripheral.

The pull-up/down and matching design recommendations for the I2S2 interface are as follows:

Signal	Internal Pull	Connection Method	Description
I2S2_MCLK	Pull Down	Series Connect	I2S system clock output
I2S2_SCLK_TX	Pull Down	Series Connect	I2S continuous serial clock (TX, related to Audio Play)
I2S2_LRCK_TX	Pull Down	Series Connect	I2S frame clock for channel selection (TX, related to Audio Play)
I2S2_SDO0	Pull Down	Direct Connection	I2S serial data 0 output

Signal	Internal Pull	Connection Method	Description
I2S2_SCLK_RX	Pull Down	Series Connect	I2S continuous serial clock (RX, related to Audio Play)
I2S2_LRCK_RX	Pull Down	Series Connect	I2S frame clock for channel selection (RX, related to Audio Record)
I2S2_SDI0	Pull Down	Direct Connection	I2S serial data 0 input

3.13 SARADC

The RK3566 microcontroller includes a SARADC (Successive Approximation Register Analog-to-Digital Converter) controller, which offers four SARADC inputs. The SARADC_VIN0 input serves as the key value sampling port and is also multiplexed as the Recovery mode button (LOADER default setting support).

By default, SARADC_VIN0 is pulled up to VCCA_1V8 through a 10k resistor, resulting in a high voltage level of 1.8V. During normal operation, when no key action is detected and the system is already flashed with firmware, the system boots directly upon power-up. However, if the Recovery mode button is pressed during system startup, SARADC_VIN0 is pulled low (0V), causing the RK3566 to enter the Rockusb Recovery flashing mode. Once the PC recognizes the USB device, releasing the button restores SARADC_VIN0 to the high voltage level (1.8V), enabling firmware flashing. Therefore, even if the Recovery mode button SARADC_VIN0 is not utilized, it is recommended to retain the 10k pull-up resistor on SARADC_VIN0 to ensure default normal startup detection.

The SARADC on the RK3566 supports a sampling range of 0-1.8V with a 10-bit precision. The keypad array can be connected in parallel, allowing for multi-key input by adjusting the voltage divider ratio through adding or removing keys and adjusting the resistors. In the design, it is important to ensure that the voltage difference between any two key values is greater than +/-35, which means that the center voltage difference must be greater than 123mV.

For proper operation, decoupling capacitors for the SARADC controller's power supply should be placed near the pins. SARADC inputs are analog signals and require proper routing protection. It is recommended to maintain a minimum distance of 3W (where W is the width of the routing) between SARADC signals and other signals. If possible, implementing ground shielding is beneficial. Additionally, when using SARADC for key collection, it is important to implement ESD protection near the keys and apply debounce measures to the key signal input. For detailed circuit information, please refer to the schematic.

The recommended SARADC interface design is as follows:

Signal	Connection	Description
SARADC_VIN0	Direct connection	Connected externally through a 10K pull-up to VCCA_1V8. Connect near the chip pin and add a 1nF capacitor. Typically used for key collection and determining the state of the Recovery mode.
SARADC_VIN[3:1]	Direct connection	Connect near the chip pin and add a 1nF capacitor. Can be flexibly used for various analog signal acquisition purposes.

4 Mechanical

The Radxa CM3 is a compact module measuring 40 × 55mm. The module itself has a depth of 4.7mm (FIXME), but when connected, the overall height will be either 5.078mm or 6.578mm (FIXME) depending on the chosen stacking height.

Here are the mechanical specifications:

- 4 × M2.5 Mounting holes, located 3.5mm inset from the module edge.
- PCB thickness is 1.2mm ± 10%.
- The height of the RK3566 SoC, including solder balls, is 2.378mm ± 0.11mm.

The following figures provide a visual representation of the Radxa CM3's mechanical form factor. All dimensions are given in millimeters (mm).

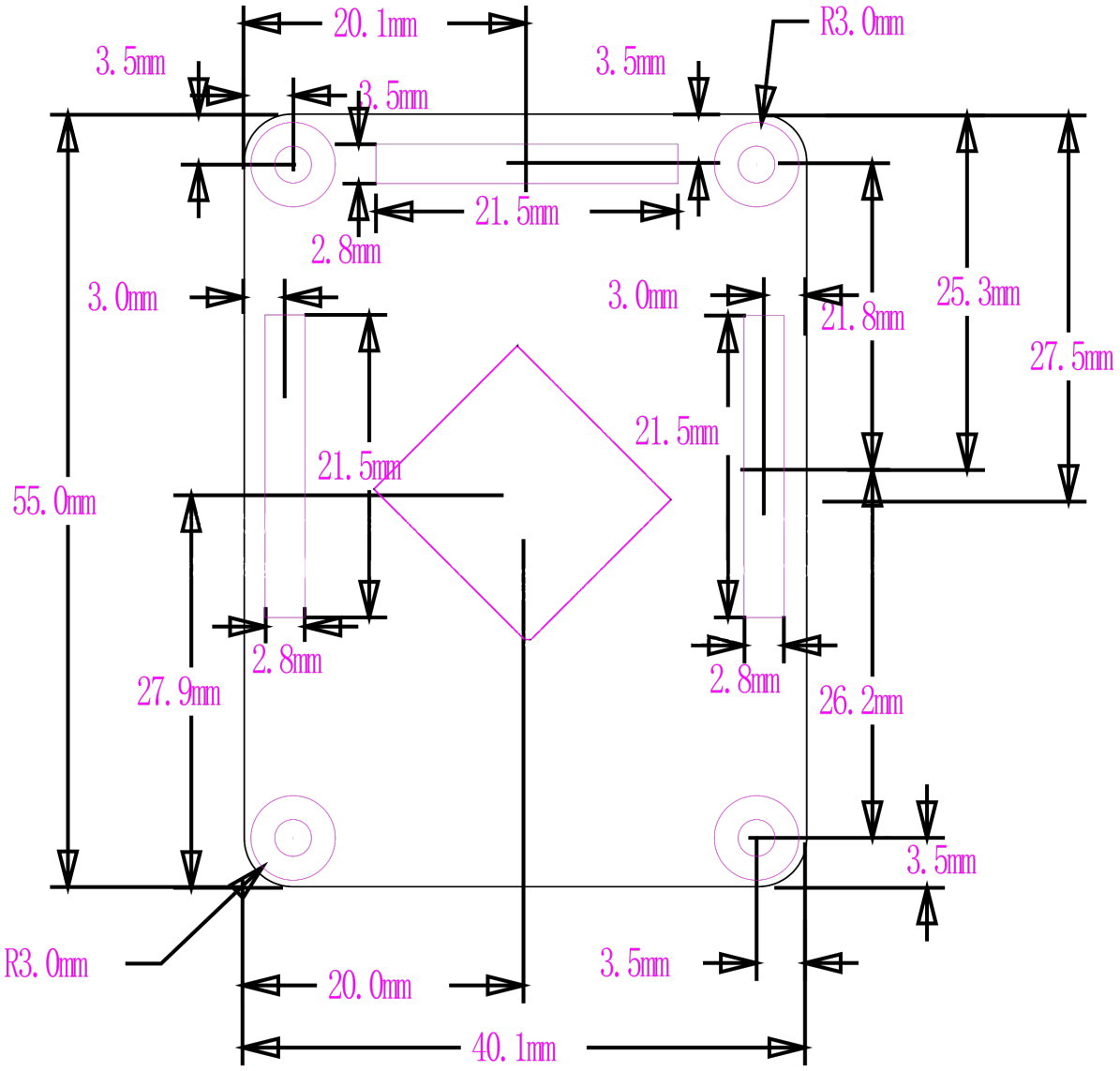

Figure 13: *Radxa CM3 Dimensions*

Note:
Please note that the location and arrangement of components on the Compute Module may undergo slight changes over time to accommodate cost and manufacturing considerations. However, the maximum component heights and PCB thickness will remain as specified.

4.1 Handling

When assembling a Radxa CM3 onto a carrier board, such as the Radxa CM3 IO board, it is crucial to follow proper handling procedures to ensure the integrity of the components and connectors. Here are detailed instructions for installing and removing the CM3:

4.1.1 Installing the Radxa CM3 onto the Carrier Board:

1. Ensure that both the Radxa CM3 and the carrier board are powered off before proceeding with the installation.
2. Align the Radxa CM3 module with the connector on the carrier board, taking care to match the corresponding pin configurations.
3. Gently lower the Radxa CM3 onto the connector, ensuring that it is properly aligned and seated.
4. Apply even and gentle pressure along the edges of the Radxa CM3, gradually pressing it down onto the connector. Take care not to exert excessive force on any specific component or area, as this can lead to damage.
5. Once the Radxa CM3 is securely mounted, visually inspect the connection to ensure proper alignment and contact between the module and the carrier board.

4.1.2 Removing the Radxa CM3 from the Carrier Board:

1. Power off the Radxa CM3 and the carrier board before starting the removal process.
2. Identify the third connector on the Radxa CM3, located on the edge opposite to the PCB edge used for handling.
3. Firmly grip the PCB edge of the third connector using your thumb and index finger, applying an equal amount of pressure on both sides.
4. Slowly and steadily pull the Radxa CM3 vertically, away from the connector on the carrier board. Ensure that the motion is smooth and straight, without any lateral or twisting force.
5. Continue pulling until the Radxa CM3 is completely detached from the connector. Take care not to bend or damage any of the pins or components during this process.
6. Once the Radxa CM3 is removed, carefully inspect the connector and the module for any signs of damage or misalignment. If any issues are detected, consult the appropriate documentation or seek technical assistance.

Improper handling during the installation or removal process can result in permanent damage to the connectors. To ensure consistent and reliable installation, especially in production environments, we strongly recommend using a fixture specifically designed for CM3 installation and removal.

4.2 Thermal Management

To ensure optimal performance and reliability of the Radxa CM3 module, proper thermal management techniques should be employed, especially when operating under extended temperatures or in demanding conditions with maximum power usage. Here are some recommendations to enhance thermal dissipation:

1. **Thermal Conductive Gap Fillers:** Apply thermal conductive gap fillers between the shielding cover and heat-generating components on the module. These gap fillers improve thermal conductivity and help dissipate heat effectively, minimizing temperature build-up.
2. **Placement and Isolation:** Position the Radxa CM3 module away from other heat sources within the system. Avoid placing it in close proximity to components that generate high levels of heat. This reduces the risk of thermal interference and helps maintain lower operating temperatures.
3. **Mechanical Enclosure:** Select a suitable mechanical enclosure for the final product that integrates the SoC on the CM3 module. The enclosure should be designed to facilitate heat radiation. Consider incorporating special treatments or materials on the enclosure's surface to enhance its heat dissipation capability, such as using thermally conductive materials or adding heat sinks.
4. **Forced Convection Cooling:** Implement a forced convection cooling scheme to actively decrease temperature rise. This can be achieved by attaching an active heat sink with adequate cooling capacity to the top of the shielding cover. The heat sink enhances heat dissipation by utilizing airflow or fans to facilitate efficient cooling of the module.

Proper thermal management ensures that the Radxa CM3 operates within the recommended temperature range, preventing overheating and potential performance degradation. By following these guidelines, you can optimize the module's thermal performance and maintain its reliability even in challenging environmental conditions.

5 Electrical Characteristics

5.1 DC Characteristics for Digital GPIO 3.3V

Parameters	Symbol	Min	Typ	Max	Unit
Digital GPIO @3.3V					
Input Low Voltage	Vil	-0.3	NA	0.8	V
Input High Voltage	Vih	2.0	NA	VCC+0.3	V
Output Low Voltage	Vol	-0.3	NA	0.4	V
Output High Voltage	Voh	2.4	NA	VCC+0.3	V
Pullup Resistor	Rpu	16	NA	43	Kohm
Pulldown Resistor	Rpd	16	NA	43	Kohm

5.2 Electrical Characteristics for Digital GPIO 3.3V

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	10	uA
Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	10	uA
High level input current	Iih	Vin = 3.3V, pulldown disabled	NA	NA	10	uA
		Vin = 3.3V, pulldown enabled	NA	NA	10	uA
Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA

5.3 DC Characteristics for Digital GPIO 1.8V

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Digital GPIO @1.8V						
Input Low Voltage	Vil	-0.3	NA	0.35*VCC		
Input High Voltage	Vih	0.65*VCC	NA	VCC+0.3		
Output Low Voltage	Vol	-0.3	NA	0.4	V	
Output High Voltage	Voh	1.4	NA	VCC+0.3		
Pullup Resistor	Rpu	16	NA	43	Kohm	
Pulldown Resistor	Rpd	16	NA	43	Kohm	

5.4 Electrical Characteristics for Digital GPIO 1.8V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Leakage Current	Ii	Vin = 1.8V or 0V	NA	NA	10uA	uA
Tri-state Output Leakage Current	Ioz	Vout = 1.8V or 0V	NA	NA	10uA	uA
High-Level Input Current	Iih	Vin = 1.8V, pulldown disabled	NA	NA	10uA	uA
High-Level Input Current	Iih	Vin = 1.8V, pulldown enabled	NA	NA	10uA	uA
Low-Level Input Current	Iil	Vin = 0V, pullup disabled	NA	NA	10uA	uA
Low-Level Input Current	Iil	Vin = 0V, pullup enabled	NA	NA	10uA	uA

5.5 DC Characteristics for MIPI

Parameters	Symbol	Min	Typ	Max	Unit
MIPI					

Parameters	Symbol	Min	Typ	Max	Unit
Output High Voltage	Voh	1.08	1.2	1.32	V
Output Low Voltage	Vol	-50	NA	50	mV
HS TX static Common-mode voltage	VCMTX	150	200	250	mV
VCMTX mismatch when output is Differential-1 or Differential-0	ΔVCMTX(1,0)	NA	NA	5	mV
HS transmit differential voltage	VOD	140	200	270	mV
VOD mismatch when output is Differential-1 or Differential-0	ΔVOD	NA	NA	14	mV
HS output high voltage	VOHHS	NA	NA	360	mV
Single ended output impedance	ZOS	40	50	62.5	Ω
Single ended output impedance mismatch	ΔZOS	NA	NA	10	%

5.6 Electrical Characteristics for MIPI DSI

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Common-mode variations above 450 MHz	ΔVcmtx(HF)	NA	NA	15	NA	mVrms
Common-mode variations between 50MHz-450MHz	ΔVcmtx(LF)	NA	NA	25	NA	mVpeak
20%-80% rise time and fall time	Tr and Tf	NA	NA	0.3	NA	UI
			10	NA	NA	ps

5.7 Electrical Characteristics for MIPI CSI

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Vin = 0V, pullup enabled	NA	NA	NA	NA	10	uA

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	10	uA
Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	10	uA
High level input current	Iih	Vin = 1.8V, pulldown disabled	NA	NA	10	uA
		Vin = 1.8V, pulldown enabled	NA	NA	10	uA
Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
		Vin = 0V, pullup enabled	NA	NA	10	uA

5.8 DC Characteristics for LVDS

Parameters	Symbol	Min	Typ	Max	Unit
LVDS					
Output High Voltage	Voh	NA	NA	1.475	V
Output Low Voltage	Vol	925	NA	NA	mV
Output differential voltage		VOD		250	NA
Output offset voltage	Vos	1125	NA	1275	mV
Output impedance, single ended	Ro	40	NA	140	Ω
Ro mismatch between A & B	ΔRo	NA	NA	10	%
Change in	Vod	between 0 and 1		ΔVod	
Change in Vod between 0 and 1	ΔVos	NA	NA	25	mV

5.9 Electrical Characteristics for HDMI

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Electrical Characteristics for PCIe PHY						
Transmitter						
Differential p-pTx voltage swing	VTX-DIFF-PP		0.8	NA	1.2	V
Low power differential p-p Tx voltage swing	VTX-DIFF-PP-LOW		0.4	NA	1.2	V
Tx de-emphasis level ratio	RTX-DIFF-DC		80	NA	120	ohm
Single Ended Output Resistance Matching	RTX-DC-OFFSET	NA	NA	NA	5	%
The amount of voltage change allowed during Receiver Detection	VTX-RCV-DETECT	NA	NA	NA	600	mV
Output rising time for 20% to 80%	Tr	25	NA	NA	ps	
Output falling time for 20% to 80%	Tf	25	NA	NA	ps	
AC Coupling Capacitor(USB3.0/PCIE2.1)	CTX	75	NA	200	nF	
AC Coupling Capacitor(SATA3.0)	CTX	6	NA	12	nF	
Unit Interval	UI	399.88	NA	NA	400.12	ps
Input Voltage Swing	Vrxdpp-c	250	NA	1200	mV	
Input differential impedance	Rrxd-c	80	NA	120	ohm	
Single Ended input Resistance Matching	Trxd-c-ms	NA	NA	NA	5	%

5.10 Electrical Characteristics for multi-PHY

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Electrical Characteristics for PCIe PHY						
Transmitter						
Differential p-pTx voltage swing	VTX-DIFF-PP		0.8	NA	1.2	V
Low power differential p-p Tx voltage swing	VTX-DIFF-PP-LOW		0.4	NA	1.2	V
Tx de-emphasis level ratio	RTX-DIFF-DC		80	NA	120	ohm
Single Ended Output Resistance Matching	RTX-DC-OFFSET	NA	NA	NA	5	%
The amount of voltage change allowed during Receiver Detection	VTX-RCV-DETECT	NA	NA	NA	600	mV
Output rising time for 20% to 80%	Tr	25	NA	NA	ps	
Output falling time for 20% to 80%	Tf	25	NA	NA	ps	
AC Coupling Capacitor(USB3.0/PCIE2.1)	CTX	75	NA	200	nF	
AC Coupling Capacitor(SATA3.0)	CTX	6	NA	12	nF	
Unit Interval	UI	399.88	NA	NA	400.12	ps
Input Voltage Swing	Vrxdpp-c	250	NA	1200	mV	
Input differential impedance	Rrxd-c	80	NA	120	ohm	
Single Ended input Resistance Matching	Trxd-c-ms	NA	NA	NA	5	%

6 Appendix A: Troubleshooting

6.1 Hardware Checklist

1. Check if the +5V_INPUT supply is good. Ensure that the power supply is providing a stable voltage of 5V to the Radxa CM3 module. Verify the voltage using a multimeter

or a power supply tester. Any fluctuations or deviations from the expected voltage may cause instability or failure of the module.

2. Check if the green LED on the CM3 is on. The green LED indicates that the module is receiving power and is properly connected. If the LED is not illuminated, check the power supply connections, ensure the power source is active, and verify that the power input to the module is correct.
3. Plug the USB OTG into a PC and check if any USB devices are detected. Connect the CM3 with IO board to a computer using the USB OTG port and verify if the PC recognizes the device. Check the device manager or system logs to see if the CM3 is detected as a USB device. Additionally, measure the voltages of `USB_OTG0_VBUSDET` and `USB_OTG0_ID` pins on the module to ensure they are above 1V, indicating proper power and identification signals. Measure `USB_OTG0_DM`/`DP` to ensure that the USB data lines are functioning correctly, as improper communication can cause connectivity issues.
4. Verify the connections and integrity of other hardware components. Ensure that all necessary connections between the Radxa CM3 and other peripherals or components on the carrier board are secure and properly seated. Check for any loose or disconnected cables, connectors, or modules. Inspect the physical condition of the components, looking for any signs of damage or irregularities.

By following this hardware checklist, you can troubleshoot common hardware-related issues and ensure that the Radxa CM3 module and its associated components are functioning correctly.

If after following the hardware checklist the Radxa CM3 module is still not recognized or you encounter persistent issues, don't hesitate to seek further assistance. Radxa provides dedicated support channels to help resolve any technical difficulties you may encounter.

6.2 Boot Order

The Radxa CM3 supports multiple boot media options. Upon system reset, the bootrom will search for booting code in the following sequence from external storage media:

- SPI Flash (only available on SKU without eMMC)
- eMMC
- SD Card

If no bootable code is found in any of the boot media, the CM3 will enter the maskrom mode. In this mode, `USB_OTG0` will be set to device mode, waiting for commands from the host PC. The USB PID and VID of the Radxa CM3 in maskrom mode when `USB_OTG0` is connected to a PC are as follows:

```
Vid=0x2207, Pid=0x350a
```

6.3 Serial Console

The low-level debug serial console is enabled by default on the Radxa CM3 using the `UART2_TX_M0` and `UART2_RX_M0` pins. The baud rate for the serial console is set to **1500000** (1.5Mbps) with an 8n1 configuration. For instructions on setting up the serial console on a host PC, please refer to the following link: https://wiki.radxa.com/Rock3/dev/serial-console

7 Appendix B: Availability

Radxa guarantees availability Radxa CM3 until at least September 2029.

7.1 Order Info

Wireless	RAM	eMMC	SKU
No	1G	-	RM116-D1E0W0
		8G	RM116-D1E8W0
		16G	RM116-D1E16W0
		32G	RM116-D1E32W0
No	2G	-	RM116-D2E0W0
		8G	RM116-D2E8W0
		16G	RM116-D2E16W0
		32G	RM116-D2E32W0
No	4G	-	RM116-D4E0W0
		8G	RM116-D4E8W0
		16G	RM116-D4E16W0
		32G	RM116-D4E32W0
		64G	RM116-D4E64W0
		128G	RM116-D4E128W0
No	8G	-	RM116-D8E0W0
		8G	RM116-D8E8W0
		16G	RM116-D8E16W0
		32G	RM116-D8E32W0
		64G	RM116-D8E64W0
		128G	RM116-D8E128W0

Wireless	RAM	eMMC	SKU
Yes	1G	-	RM116-D1E0W2
		8G	RM116-D1E8W2
		16G	RM116-D1E16W2
		32G	RM116-D1E32W2
Yes	2G	-	RM116-D2E0W2
		8G	RM116-D2E8W2
		16G	RM116-D2E16W2
		32G	RM116-D2E32W2
Yes	4G	-	RM116-D4E0W2
		8G	RM116-D4E8W2
		16G	RM116-D4E16W2
		32G	RM116-D4E32W2
		64G	RM116-D4E64W2
		128G	RM116-D4E128W2
Yes	8G	-	RM116-D8E0W2
		8G	RM116-D8E8W2
		16G	RM116-D8E16W2
		32G	RM116-D8E32W2
		64G	RM116-D8E64W2
		128G	RM116-D8E128W2

7.2 Support

For support please see the hardware documentation section of the Radxa Wiki website and post questions to the Radxa forum.

8 Appendix C: Alternative Function

Some of the pins has up to 6 alternate functions available. The RK3566 datasheet describes these features in detail. The table below gives a quick overview of all available pin functions and the default function on the Radxa CM3 IO board.

> If use other functions than the default CM3 IO board, proper device tree or device tree overlay should be applied.

8.1 Connector 1 (J69)

Table 46: *Connector 1 (J69) pinout*

Pin Number	Function CM3 IO Board	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5
1	GND						
2	GND						
3	PHY1_MDI3+						
4	PHY1_MDI1+						
5	PHY1_MDI3-						
6	PHY1_MDI1-						
7	GND						
8	GND						
9	PHY1_MDI2-						
10	PHY1_MDI0-						
11	PHY1_MDI2+						
12	PHY1_MDI0+						
13	GND						
14	GND						
15	PHY1_LED2_Y						
16	NC						
17	PHY1_LED1_G						
18	NC						
19	PHY1_LED0_Y1						
20	EEPROM_NWP						
21	PI_NLED_ACTIVITY	GPIO4_A4	CIF_D14	EBC_SDDO14	GMAC1_TXD0_M1	UART9_TX_M2	I2S2_LRCK_TX_M1
22	GND						
23	GND						
24	PWM3_IR	GPIO0_C2	PWM3_IR	EDP_HPDIN_M1	MCU_JTAG_TMS		
25	I2S1_SDO0_M1	GPIO3_D1	CIF_D3	EBC_SDDO3	SDMMC2_D3_M0	I2S1_SDO0_M1	VOP_BT656_D3_M1
26	I2S1_LRCK_TX_M1	GPIO3_D0	CIF_D2	EBC_SDDO2	SDMMC2_D2_M0	I2S1_LRCK_TX_M1	VOP_BT656_D2_M1
27	I2S1_SDI0_M1	GPIO3_D2	CIF_D4	EBC_SDDO4	SDMMC2_CMD_M0	I2S1_SDI0_M1	VOP_BT656_D4_M1
28	SPI0_CSO_MO	GPIO0_C6	PWM7_IR	SPI0_CS0_M0			
29	I2S1_LRCK_RX_M1	GPIO4_A7	CAM_CLKOUT0	EBC_SDCE1	GMAC1_RXD0_M1	SPI3_CS1_M0	I2S1_LRCK_RX_M1
30	SPI0_MISO_MO	GPIO0_C5	PWM6	SPI0_MISO_M0			
31	PWM11	GPIO4_C0	CIF_CLKOUT	EBC_GDCLK	PWM11_IR_M1		
32	GND						
33	GND						
34	I2S1_SDO2_M1	GPIO4_B1	ISP_PRELIGHT_TRIG	EBC_SDCE3	GMAC1_RXDV_CRS_M1	I2S1_SDO2_M1	

Pin Number	Function CM3 IO Board	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5
35	I2C2_SCL_M1	GPIO4_B5	I2C2_SCL_M1	EBC_SDSHR		I2S1_SDO3_M1	
36	I2C2_SDA_M1	GPIO4_B4	I2C2_SDA_M1	EBC_GDSP		ISP_FLASH_TRIGIN	VOP_BT656_CLK_M1
37	SARADC_IN3	SARADC_VIN3					
38	SPI3_CLK_M0	GPIO4_B3	I2C4_SCL_M0	EBC_GDOE	ETH1_REFCLKO_25M_M0	SPI3_CLK_M0	I2S2_SDO_M1
39	SPI3_CSO_M0	GPIO4_A6	ISP_FLASHTRIGOUT	EBC_SDCE0	GMAC1_TXEN_M1	SPI3_CS0_M0	I2S1_SCLK_RX_M1
40	SPI3_MISO_M0	GPIO4_B0	CAM_CLKOUT1	EBC_SDCE2	GMAC1_RXD1_M1	SPI3_MISO_M0	I2S1_SDO1_M1
41	I2S1_MCLK_M1	GPIO3_C6	CIF_D0	EBC_SDDO0	SDMMC2_D0_M0	I2S1_MCLK_M1	VOP_BT656_D0_M1
42	GND						
43	GND						
44	SPI3_MOSI_M0	GPIO4_B2	I2C4_SDA_M0	EBC_VCOM	GMAC1_RXER_M1	SPI3_MOSI_M0	I2S2_SDI_M1
45	I2S1_SDI1_M1	GPIO3_D3	CIF_D5	EBC_SDDO5	SDMMC2_CLK_M0	I2S1_SDI1_M1	VOP_BT656_D5_M1
46	PMW4	GPIO0_C3	PWM4	VOP_PWM_M0	MCU_JTAG_TRSTn		
47	I2S1_SDI2_M1	GPIO3_D4	CIF_D6	EBC_SDDO6	SDMMC2_DET_M0	I2S1_SDI2_M1	VOP_BT656_D6_M1
48	PMW0_M0	GPIO0_B7	PWM0_M0	CPUAVS			
49	I2S1_SCLK_TX_M1	GPIO3_C7	CIF_D1	EBC_SDDO1	SDMMC2_D1_M0	I2S1_SCLK_TX_M1	VOP_BT656_D1_M1
50	PMW0_M1	GPIO0_C7	HDMITX_CEC_M1	PWM0_M1	UART0_CTSn		
51	UART2_RX	GPIO0_D0	UART2_RX_M0				
52	GND						
53	GND						
54	I2S1_SDI3_M1	GPIO3_D5	CIF_D7	EBC_SDDO7	SDMMC2_PWREN_M0	I2S1_SDI3_M1	VOP_BT656_D7_M1
55	UART2_TX	GPIO0_D1	UART2_TX_M0				
56	I2C2_SCL_MO	GPIO0_B5	I2C2_SCL_M0	SPI0_CLK_M0	PCIE20_WAKEn_M0	PWM1_M1	
57	SDMMC0_CLK	GPIO2_A2	SDMMC0_CLK	TEST_CLKOUT	UART5_TX_M0		
58	I2C2_SDA_MO	GPIO0_B6	I2C2_SDA_M0	SPI0_MOSI_M0	PCIE20_PERSTn_M0	PWM2_M1	
59	GND						
60	GND						
61	SDMMC0_D3	GPIO2_A0	SDMMC0_D3	ARM_JTAG_TMS	UART5_RTSn_M0		
62	SDMMC0_CMD	GPIO2_A1	SDMMC0_CMD	PWM10_M1	UART5_RX_M0		
63	SDMMC0_D0	GPIO1_D5	SDMMC0_D0	UART2_TX_M1	UART6_TX_M1	PWM8_M1	
64	NC						
65	GND						
66	GND						
67	SDMMC0_D1	GPIO1_D6	SDMMC0_D1	UART2_RX_M1	UART6_RX_M1	PWM9_M1	
68	NC						
69	SDMMC0_D2	GPIO1_D7	SDMMC0_D2	ARM_JTAG_TCK	UART5_CTSn_M0		
70	NC						
71	GND						
72	NC						
73	NC						
74	GND						
75	SDMMC_PWREN	GPIO0_A5	SDMMC0_PWREN	SATA_MP_SWITCH	PCIE20_CLKREQn_M0		
76	SDMMC0_DET_L	GPIO0_A4	SDMMC0_DET	SATA_CP_DET			
77	+5V_INPUT						
78	GPIO_VREF						
79	+5V_INPUT						
80	I2C0_SCL_PMIC	GPIO0_B1	I2C0_SCL				
81	+5V_INPUT						
82	I2C0_SDA_PMIC	GPIO0_B2	I2C0_SDA				
83	+5V_INPUT						
84	+3V3						
85	+5V_INPUT						
86	+3V3						
87	+5V_INPUT						
88	+1V8						

Pin Number	Function CM3 IO Board	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5
89	WL_NDIS	GPIO4_B6	CIF_HREF	EBC_SDLE	GMAC1_MDC_M1	UART1_RTSn_M1	I2S2_MCLK_M1
90	+1V8						
91	BT_NDIS	GPIO4_A5	CIF_D15	EBC_SDDO15	GMAC1_TXD1_M1	UART9_RX_M2	I2S2_LRCK_RX_M1
92	PMIC_SLEEP_H	GPIO0_A2	PMIC_SLEEP	TSADC_SHUT_M1			
93	NC						
94	NC						
95	NPWR_LED	GPIO4_B7	CIF_VSYNC	EBC_SDOE	GMAC1_MDIO_M1	I2S2_SCLK_TX_M1	
96	NC						
97	CAM_GPIO	GPIO4_C1	CIF_CLKIN	EBC_SDCLK	GMAC1_MCLK_M1	UART1_CTSn_M1	I2S2_SCLK_RX_M1
98	GND						
99	PWRON_KEY						
100	PMIC_RESET_KEY						

8.2 Connector 2 (J68)

Table 47: *Connector 2 (J68) pinout*

Pin Number	Function CM3 IO Board	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5
101	USB_OTG0_ID	USB_OTG0_ID					
102	PCIE20_CLKREQN_M2	GPIO1_B0	I2S1_SDO1_M0	I2S1_SDI3_M0	PDM_SDI3_M0	PCIE20_CLKREQn_M2	
103	USB_OTG0_DM	USB_OTG0_DM					
104	NC						
105	USB_OTG0_DP	USB_OTG0_DP					
106	NC						
107	GND						
108	GND						
109	PCIE_NRST	GPIO1_B2	I2S1_SDO3_M0	I2S1_SDI1_M0	PDM_SDI1_M0	PCIE20_PERSTn_M2	
110	PCIE20_REFCLKP	PCIE20_REFCLKP					
111	NC						
112	PCIE20_REFCLKN	PCIE20_REFCLKN					
113	GND						
114	GND						
115	MIPI_CSI_RX_D0N	MIPI_CSI_RX_D0N					
116	PCIE20_RXP	PCIE20_RXP	SATA2_RXP				
117	MIPI_CSI_RX_D0P	MIPI_CSI_RX_D0P					
118	PCIE20_RXN	PCIE20_RXN	SATA2_RXN				
119	GND						
120	GND						
121	MIPI_CSI_RX_D1N	MIPI_CSI_RX_D1N					
122	PCIE20_TXP	PCIE20_TXP	SATA2_TXP				
123	MIPI_CSI_RX_D1P	MIPI_CSI_RX_D1P					
124	PCIE20_TXN	PCIE20_TXN	SATA2_TXN				
125	GND						
126	GND						
127	MIPI_CSI_RX_CLK0N	MIPI_CSI_RX_CLK0N					
128	MIPI_CSI_RX_D2N	MIPI_CSI_RX_D2N					
129	MIPI_CSI_RX_CLK0P	MIPI_CSI_RX_CLK0P					
130	MIPI_CSI_RX_D2P	MIPI_CSI_RX_D2P					
131	GND						
132	GND						

Pin Number	Function CM3 IO Board	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5
133	NC						
134	MIPI_CSI_RX_D3N	MIPI_CSI_RX_D3N					
135	NC						
136	MIPI_CSI_RX_D3P	MIPI_CSI_RX_D3P					
137	GND						
138	GND						
139	NC						
140	MIPI_CSI_RX_CLK1N	MIPI_CSI_RX_CLK1N					
141	NC						
142	MIPI_CSI_RX_CLK1P	MIPI_CSI_RX_CLK1P					
143	NC						
144	GND						
145	NC						
146	NC						
147	NC						
148	NC						
149	NC						
150	GND						
151	HDMI_TX_CEC_PORT	GPIO4_D1	HDMITX_CEC_M0	SPI3_CS1_M1			
152	NC						
153	HDMI_TX_HPD_PORT	HDMI_TX_HPDIN					
154	NC						
155	GND						
156	GND						
157	MIPI_DSI_TX0_D0N	MIPI_DSI_TX0_D0N	LVDS_TX0_D0N				
158	NC						
159	MIPI_DSI_TX0_D0P	MIPI_DSI_TX0_D0P	LVDS_TX0_D0P				
160	NC						
161	GND						
162	GND						
163	MIPI_DSI_TX0_D1N	MIPI_DSI_TX0_D1N	LVDS_TX0_D1N				
164	NC						
165	MIPI_DSI_TX0_D1P	MIPI_DSI_TX0_D1P	LVDS_TX0_D1P				
166	NC						
167	GND						
168	GND						
169	MIPI_DSI_TX0_CLKN	MIPI_DSI_TX0_CLKN	LVDS_TX0_CLKN				
170	HDMI_TX2P_PORT	HDMI_TX_D2P					
171	MIPI_DSI_TX0_CLKP	MIPI_DSI_TX0_CLKP	LVDS_TX0_CLKP				
172	HDMI_TX2N_PORT	HDMI_TX_D2N					
173	GND						
174	GND						
175	MIPI_DSI_TX1_D0N	MIPI_DSI_TX1_D0N					
176	HDMI_TX1P_PORT	HDMI_TX_D1P					
177	MIPI_DSI_TX1_D0P	MIPI_DSI_TX1_D0P					
178	HDMI_TX1N_PORT	HDMI_TX_D1N					
179	GND						
180	GND						
181	MIPI_DSI_TX1_D1N	MIPI_DSI_TX1_D1N					
182	HDMI_TX0P_PORT	HDMI_TX_D0P					
183	MIPI_DSI_TX1_D1P	MIPI_DSI_TX1_D1P					
184	HDMI_TX0N_PORT	HDMI_TX_D0N					
185	GND						
186	GND						

Pin Number	Function CM3 IO Board	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5
187	MIPI_DSI_TX1_CLKN	MIPI_DSI_TX1_CLKN					
188	HDMI_TXCLKP_PORT	HDMI_TX_CLKP					
189	MIPI_DSI_TX1_CLKP	MIPI_DSI_TX1_CLKP					
190	HDMI_TXCLKN_PORT	HDMI_TX_CLKN					
191	GND						
192	GND						
193	MIPI_DSI_TX1_D2N	MIPI_DSI_TX1_D2N					
194	MIPI_DSI_TX1_D3N	MIPI_DSI_TX1_D3N					
195	MIPI_DSI_TX1_D2P	MIPI_DSI_TX1_D2P					
196	MIPI_DSI_TX1_D3P	MIPI_DSI_TX1_D3P					
197	GND						
198	GND						
199	HDMI_TXDDC_SDA_PORT	GPIO4_D0	HDMITX_SDA	I2C5_SDA_M1			
200	HDMI_TXDDC_SCL_PORT	GPIO4_C7	HDMITX_SCL	I2C5_SCL_M1			

8.3 Connector 3 (J1)

Table 48: *Connector 3 (J1) pinout*

Pin Number	Function CM3 IO Board	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5
1	GND						
2	GND						
3	MIPI_DSI_TX0_D2N	MIPI_DSI_TX0_D2N	LVDS_TX0_D2N				
4	GPIO3_A1	GPIO3_A1	VOP_BT1120_D0	SPI1_CS0_M1	SDMMC2_D0_M1		
5	MIPI_DSI_TX0_D2P	MIPI_DSI_TX0_D2P	LVDS_TX0_D2P				
6	GPIO3_B4	GPIO3_B4	VOP_BT1120_D10	GMAC1_RXER_M0	I2C5_SDA_M0	PDM_SDI1_M2	
7	GND						
8	GPIO3_C1	GPIO3_C1	VOP_BT1120_D13	SPI1_MOSI_M1	PCIE20_PERSTn_M1	I2S1_SDO2_M2	
9	MIPI_DSI_TX0_D3N	MIPI_DSI_TX0_D3N	LVDS_TX0_D3N				
10	GPIO3_C2	GPIO3_C2	VOP_BT1120_D14	SPI1_MISO_M1	UART5_TX_M1	I2S1_SDO3_M2	
11	MIPI_DSI_TX0_D3P	MIPI_DSI_TX0_D3P	LVDS_TX0_D3P				
12	GPIO3_C3	GPIO3_C3	VOP_BT1120_D15	SPI1_CLK_M1	UART5_RX_M1	I2S1_SCLK_RX_M2	
13	GND						
14	PCIE_PWREN_H	GPIO0_D3					
15	EDP_TX_D0P	EDP_TX_D0P					
16	NC						
17	EDP_TX_D0N	EDP_TX_D0N					
18	GPIO_D5	GPIO0_D5					
19	GND						
20	GPIO_D6	GPIO0_D6					
21	EDP_TX_D1P	EDP_TX_D1P					
22	GND						
23	EDP_TX_D1N	EDP_TX_D1N					
24	GPIO2_C6	GPIO2_C6	CLK32K_OUT1	UART8_RX_M0	SPI1_CS1_M0		
25	GND						
26	SARADC_VIN0_KEY/RECOVERY	SARADC_VIN0					
27	EDP_TX_D2P	EDP_TX_D2P					
28	SARADC_VIN1_HW_ID	SARADC_VIN1					
29	EDP_TX_D2N	EDP_TX_D2N					
30	SARADC_VIN2_HP_HOOK						

Pin Number	Function CM3 IO Board	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5
31	GND						
32	GND						
33	EDP_TX_D3P	EDP_TX_D3P					
34	4G_DISABLE	GPIO4_C5	PWM12_M1	SPI3_MISO_M1	SATA1_ACT_LED	UART9_TX_M1	I2S3_SDO_M1
35	EDP_TX_D3N	EDP_TX_D3N					
36	HP_DET_L	GPIO4_C6	PWM13_M1	SPI3_CS0_M1	SATA0_ACT_LED	UART9_RX_M1	I2S3_SDI_M1
37	GND						
38	PDM_SDI2_M0_ADC	GPIO1_B1	I2S1_SDO2_M0	I2S1_SDI2_M0	PDM_SDI2_M0	PCIE20_WAKEn_M2	
39	EDP_TX_AUXP	EDP_TX_AUXP					
40	PDM_CLK1_M0	GPIO1_A4	I2S1_SCLK_RX_M0	UART4_RX_M0	PDM_CLK1_M0	SPDIF_TX_M0	
41	EDP_TX_AUXN	EDP_TX_AUXN					
42	GND						
43	GND						
44	I2C3_SCL_ACODEC	GPIO1_A1	I2C3_SCL_M0	UART3_TX_M0		AUDIOPWM_LOUT_N	
45	USB3_HOST1_DP	USB_HOST1_DP					
46	I2C3_SDA_ACODEC	GPIO1_A0	I2C3_SDA_M0	UART3_RX_M0		AUDIOPWM_LOUT_P	
47	USB3_HOST1_DM	USB_HOST1_DM					
48	GND						
49	GND						
50	HPL_OUT						
51	USB3_HOST1_SSTXP	USB3_HOST1_SSTXP	SATA1_TXP				
52	HP_SNS						
53	USB3_HOST1_SSTXN	USB3_HOST1_SSTXN	SATA1_TXN				
54	HPR_OUT						
55	GND						
56	GND						
57	USB3_HOST1_SSRXP	USB3_HOST1_SSRXP	SATA1_RXP				
58	SPKN_OUT						
59	USB3_HOST1_SSRXN	USB3_HOST1_SSRXN	SATA1_RXN				
60	SPKP_OUT						
61	GND						
62	GND						
63	USB2_HOST2_DP	USB_HOST2_DP					
64	MIC1_IN						
65	USB2_HOST2_DM	USB_HOST2_DM					
66	MIC2_IN						
67	GND						
68	GND						
69	USB2_HOST3_DP	USB_HOST3_DP					
70	SPDIF_TX_M2	GPIO4_C4	EDP_HPDIN_M0	SPDIF_TX_M2	SATA2_ACT_LED	I2S3_LRCK_M1	
71	USB2_HOST3_DM	USB_HOST3_DM					
72	GND						
73	GND						
74	WIFI_PWREN	GPIO0_A0	REFCLK_OUT				
75	PDM_CLK0_M1	GPIO3_D6	CIF_D8	EBC_SDDO8	GMAC1_TXD2_M1	UART1_TX_M1	PDM_CLK0_M1
76	GND						
77	PDM_SDIO_M1	GPIO3_D7	CIF_D9	EBC_SDDO9	GMAC1_TXD3_M1	UART1_RX_M1	PDM_SDI0_M1
78	VCC_BAT-						
79	PDM_CLK1_M1	GPIO4_A0	CIF_D10	EBC_SDDO10	GMAC1_TXCLK_M1	PDM_CLK1_M1	
80	VCC_BAT-						
81	PDM_SDI1_M1	GPIO4_A1	CIF_D11	EBC_SDDO11	GMAC1_RXD2_M1	PDM_SDI1_M1	
82	VCC_BAT-						
83	PDM_SDI2_M1	GPIO4_A2	CIF_D12	EBC_SDDO12	GMAC1_RXD3_M1	UART7_TX_M2	PDM_SDI2_M1
84	VCC_BAT+						

Pin Number	Function CM3 IO Board	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5
85	PDM_SDI3_M1	GPIO4_A3	CIF_D13	EBC_SDDO13	GMAC1_RXCLK_M1	UART7_RX_M2	PDM_SDI3_M1
86	VCC_BAT+						
87	GPIO_B3	GPIO0_B3	I2C1_SCL		MCU_JTAG_TDO		
88	VCC_BAT+						
89	GPIO_B4	GPIO0_B4	I2C1_SDA		PCIE20_BUTTONRSTn	MCU_JTAG_TCK	
90	TS						
91	NC						
92	VCC_SD						
93	GPIO_C1	GPIO0_C1	PWM2_M0	NPUAVS	UART0_TX	MCU_JTAG_TDI	
94	USB_5V_IN						
95	GPIO_C4	GPIO0_C4	PWM5	SPI0_CS1_M0	UART0_RTSn		
96	USB_5V_IN						
97	USB_OTG0_VBUSDET	USB_OTG0_VBUSDET					
98	USB_5V_IN						
99	GND						
100	GND						

9 Appendix D: Abbreviations and Definitions

Abbreviation	Definition
B2B	Board-to-Board: Refers to a connection or configuration where two circuit boards are directly connected to each other without any intermediary components or interfaces in between.
Boot Media	The storage device from which the system boots or initializes.
Bootrom	A small piece of code located in the read-only memory of a device that is responsible for the initial boot process.
Baud Rate	The number of signal changes per second in a communication channel. It represents the transmission speed of data.
CM3	Radxa CM3: The Radxa CM3 is a compact compute module developed by Radxa, featuring a powerful SoC and various integrated components for embedded computing applications.
Debug Serial Console	A communication interface used for low-level debugging and accessing system information.
eDP	Embedded DisplayPort: A display interface standard primarily used in laptops, tablets, and other embedded systems for connecting the display panel to the graphics controller.
eMMC	Embedded MultiMediaCard: A type of non-volatile flash storage commonly used in portable electronic devices, providing high-speed data access and reliable storage capabilities.
HDMI	High-Definition Multimedia Interface: A digital audio/video interface used for transmitting high-quality uncompressed audio and video signals between devices such as TVs, monitors, and projectors.
I2C	Inter-Integrated Circuit: A serial communication protocol that allows multiple devices to communicate with each other using a shared bus.
I2S	Inter-IC Sound: A serial bus interface used for transmitting digital audio data between integrated circuits, typically for connecting audio devices such as microphones, speakers, and digital audio converters.
Maskrom Mode	A mode in which the device enters when there is no bootable code found in the boot media. It allows the device to be recognized by a host PC for firmware flashing or other operations.
PCB	Printed Circuit Board: A board made of insulating material with conductive pathways etched or printed onto it to connect electronic components and provide mechanical support for circuitry.
PCIe	Peripheral Component Interconnect Express: A high-speed serial computer expansion bus standard used for connecting various peripheral devices to a computer motherboard.
PID	Product ID: A unique identifier assigned to a specific product, often used in combination with the Vendor ID (VID) to identify and differentiate devices in computer systems or networks.
SKU	Stock Keeping Unit: A unique identifier assigned to a particular product or item for inventory tracking and management purposes. It is used to distinguish between different variations or configurations of the same product.
SoC	System-on-a-Chip: An integrated circuit that integrates multiple components of a computer or electronic system, including a microprocessor, memory, input/output interfaces, and other necessary circuits, onto a single chip.
UART	Universal Asynchronous Receiver-Transmitter: A hardware component used for serial communication.
USB	Universal Serial Bus: A popular standard for connecting various peripherals and devices to a computer system.
VID	Vendor ID: A unique identifier assigned to a specific manufacturer or vendor, often used in combination with the Product ID (PID) to identify and differentiate devices in computer systems or networks.